National Semiconductor

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Hardware Reference Manual

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Rack-Mount Computer Systems

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MICROSYSTEM 6600™

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Rack-Mount Computer Systems
Hardware Reference Manual

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PREFACE

This manual presents an overview of the MICROSYSTEM 6600™ hardware. The information describes the overall system capabilities and how the integrated hardware/software features are structured to meet the needs for a variety of user applications.

The contents of this manual are oriented to introduce the system capability to a potential user who would install and operate the equipment.

A list of additional manuals is included for user reference. These manuals contain expanded coverage of the software structure and extended details of hardware functions. These manuals are intended to provide in-depth background information for the user who is concerned with either the software operating system or board-level circuit functions.

The material contained in this manual is for information only and is subject to change without notice.

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Chapter 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The MICROSYSTEM 6600 is a microcomputer designed to meet the small system needs of business and industrial users. It is a growth-oriented system using proven hardware and an industry standard software operating system.

The MICROSYSTEM 6600 is configured from proven National Semiconductor Board Level Computer (BLC) products. The system is offered in two basic configurations. Both configurations are rack-mounted and consist of two modules: the rack-mounted microcomputer (logic board) module and the rack-mounted diskette drive module. One configuration consists of a four-slot logic board module and a diskette drive module; the other consists of an eight-slot logic board module and diskette drive module.

Model number MSC-6601 identifies the four-slot configuration and model number MSC-6605 identifies the eight-slot configuration. Table 1-1 lists the BLC products supplied with each model.

1.2 FEATURES

1.2.1 Hardware Features

The MICROSYSTEM 6600 offers the following hardware features:

- Rack-Mounted Microcomputer Module with CPU, diskette controller, and 64K bytes of RAM memory
- Rack-Mounted Diskette Drive Module, with two drives and an internal power supply
- All necessary fans, cables, and connectors
- MULTIBUS* system compatible backplanes and card slots for mounting from one to five additional BLC products, depending on selected configuration
- DC power sufficient to support the maximum complement of additional BLC products
- Two RS232C compatible I/O ports
- Two parallel I/O ports

* MULTIBUS is a trademark of the INTEL Corporation

TABLE 1-1 MICROSYSTEM 6600 MODEL IDENTIFICATION CHART

MODEL NUMBER	EQUIPMENT PROVIDED							
	DISKETTE DRIVE MODULE	SYSTEM PROCESSOR BOARD Z80 CPU	BLC-8222	BLC-064	BLC-635	BLC-665	BLC-604	BLC-614
MSC-6601	X	X	X	X	X		X	
MSC-6605	X	X	X	X		X	X	X

1.2.2 Software Features

- CP/M operating system
- IBM-compatible disk format
- Comprehensive file management system
- Text editor
- 8080-compatible assembler
- Debugger

1.2.3 Peripherals

The standard MICROSYSTEM 6600 feature package supports the following optional peripherals:

- CRT/KB terminal
- Centronics printer

1.3 SYSTEM CONFIGURATION

Each model of the MICROSYSTEM 6600 consists of a rack-mounted microcomputer module, a rack-mounted diskette drive module, and a support package consisting of a software operating system, diagnostic software, and technical manuals.

The rack-mount modules have individual power supplies that operate from the available commercial AC power. A single 50-conductor ribbon cable provides all necessary address, data, and control signal connections between the modules. Additional connectors mounted on the rear panel of the microcomputer module provide for optional I/O devices such as printers and terminals. The location of these connectors is given in Chapter 3.

1.3.1 Microcomputer Module Configuration

Two microcomputer modules are available, one with four card slots and the other with eight card slots. The card slots are used to mount BLC-type printed circuit boards. Each module is equipped with two standard SERIES/80 BLC boards and a Z80-based Processor board.

The SERIES/80 boards are:

BLC-064	64K RAM Board
BLC-8222	Flexible Disk Controller Board

The power supply provided with each microcomputer module has sufficient capacity to power the three standard boards and up to the maximum number of optional BLC boards (one in the four slot unit and five in the eight slot unit).

1.3.2 Diskette Drive Module Configuration

The Diskette Drive Module includes two standard-size (8-inch), single-sided, flexible disk drives, drive power supply, and required power harness and signal cables. The disk drives are designated as drive A and drive B.

1.3.3 Support Package Configuration

The MICROSYSTEM 6600 support package includes the National Semiconductor CP/M operating system, the MICROSYSTEM 6600 diagnostic program, and two system-level technical manuals. The operating system and diagnostics are provided on separate flexible disks. A boot strap loader, provided as firmware on the CPU board, provides for program loading from the disk drives to system memory.

The system level technical manuals are

MSC-6601/MSC-6605 HARDWARE REFERENCE MANUAL
MICROSYSTEM 6600 SOFTWARE REFERENCE MANUAL

1.4 AVAILABLE CONFIGURATIONS

The MICROSYSTEM 6600 is optionally provided with either a four-slot or an eight-slot microcomputer module. The four-slot module provides space for one additional BLC-type printed circuit board. The eight-slot module provides space for up to five additional BLC-type printed circuit boards.
The National Semiconductor Corporation publication, "Microcomputer Systems Series/80 Databook", provides a listing of available BLC products.

1.5 DOCUMENTATION

1.5.1 Required Documentation

The following documents are required to install, operate, and maintain the MICROSYSTEM 6600:

- MSC-6601/MSC-6605 -- Hardware Reference Manual, Document Number 420306559-001
- MICROSYSTEM 6600 -- Software Reference Manual, Document Number 420306395-001

1.5.2 Related Documentation

The following documents contain information related to the MICROSYSTEM 6600 and are referenced in the required documentation:

- BLC-635 Power Supply -- User's Manual, Document Number 420305489-001
- BLC-665 Power Supply -- User's Manual, Document Number 420302220-001
- BLC-8016, 032, 048, 064 16K/32K/48K/64K RAM Board -- Hardware Reference Manual, Document Number 420305529-001
- BLC-8222 Double/Single Density Floppy Disk Controller Board -- Hardware Reference Manual, Document Number 420305804-001

Chapter 2

SPECIFICATIONS

2.1 GENERAL INFORMATION

This chapter describes the physical, environmental, and power specifications for the MICROSYSTEM 6600 rack-mount modules. Detailed specifications for board-level timing conditions and AC/DC characteristics are provided in the SERIES/80 hardware reference manuals listed in Section 1.5.2 and in Chapter 5.

2.2 FOUR-SLOT MICROCOMPUTER MODULE - MSC-6601

Front Panel Switches:	Power ON/OFF, RESET
Input Power:	100, 115, 230 VAC ± 10%, 47-63Hz
Fusing:	100, 115 VAC -- 3A, Slo-Blo 230 VAC -- 1.5A, Slo-Blo
Environmental:	Temperature -- 0-55°C Humidity -- 0-90%, non-condensing
Physical:	Height -- 3.5 inches Width -- 19.0 inches Depth -- 20.0 inches Weight -- 37.0 pounds

2.3 EIGHT-SLOT MICROCOMPUTER MODULE - MSC-6605

Front Panel Switches:	Power ON/OFF, RESET
Input Power:	100, 115, 230 VAC ± 10%, 47-63Hz
Fusing:	100, 115 VAC -- 6A, Slo-Blo 230 VAC -- 3A, Slo-Blo
Environmental:	Temperature -- 0-55°C Humidity -- 0-90%, non-condensing
Physical:	Height -- 7.0 inches Width -- 19.0 inches Depth -- 20.0 inches Weight -- 49.0 pounds

2.4 DISKETTE DRIVE MODULE

2.4.1 Physical Specifications

Front Panel Switches:	Power ON/OFF
Input Power:	100, 115, VAC ± 10%, 60Hz ± 0.5Hz 100, 230, VAC ± 10%, 50Hz ± 0.5Hz
Fusing:	100, 115 VAC -- 2A, Slo-Blo 230 VAC -- 1A, Slo-Blo
Environmental:	Temperature -- 4.4°C - 46.1°C Humidity -- 20% - 80%
Physical:	Height -- 7.0 inches Width -- 19.0 inches Depth -- 20.0 inches Weight -- 54.0 pounds

2.4.2 Electrical Specifications

Sector Type:	Soft Sectored
Data Encoding:	FM (Single Density) MFM (Double Density)
Bytes Per Sector:	128, 256, or 512 Bytes (Software Selectable)
Storage Capacity:	FM -- 400K bytes/diskette MFM -- 800K bytes/diskette
Data Transfer Rate:	FM -- 250K bytes/sec MFM -- 500K bytes/sec
Drive Latency:	83 msec (Avg.)
Drive Access Time:	Track to Track -- 8 msec Average -- 260 msec
Head Load Time:	35 msec

Chapter 3

SYSTEM INSTALLATION

3.1 GENERAL INFORMATION

This chapter describes how to unpack, inspect, and install the MICROSYSTEM 6600. On-site operational checks are included. Complete information, from preparing the installation site to running diagnostics, is included.

MICROSYSTEM 6600 components are assembled and packaged to meet each customer's power requirements and hardware/software options. Before installation, each component must be inspected to verify the proper configuration.

3.2 SITE PREPARATION

The MICROSYSTEM 6600 modules are designed to fit standard 19" equipment racks. Because of the weight of the modules, the use of equipment slides and/or equipment rails, in addition to securing the front panels to the equipment racks, is strongly recommended. Appendix A contains outline drawings of the MICROSYSTEM 6600 modules. These drawings give equipment dimensions, show the location of front panel cutouts for mounting screws, and the location of pre-drilled holes on the side panels for mounting equipment slides.

3.2.1 Equipment Location

The cable provided for connecting the microcomputer module to the diskette drive module is 24 inches long. This should be considered a restriction when planning the location of the modules. Otherwise, the modules can be located one on top of the other or side by side. Orientation of the modules is not critical.

3.2.2 Clearance Requirements

Sufficient clearance must be maintained at the rear of the modules to allow for the power and signal cables and their connectors. Side clearance must allow for unrestricted air flow for the cooling fans. Refer to the physical specifications in Chapter 2 and the outline drawings in Appendix A for the module dimensions.

CAUTION

Conditions within closed equipment racks, such as chimney effect, can result in local hot spots. When the MICROSYSTEM 6600 is installed in a closed equipment rack, temperature tests should be made under operating conditions, to ensure the environmental specifications outlined in Chapter 2 are met. This is especially true if other heat-producing equipment is located in the same rack.

3.2.3 Power Considerations

Each module is shipped with an UL(VDE) approved 7-foot long AC power cord. The equipment rack should provide, or be within 7 feet of, a suitable source of AC power.

3.3 UNPACKING AND INVENTORY

The MICROSYSTEM 6600 is shipped in three separate boxes, one containing the microcomputer module, another containing the diskette drive module, and a third containing the equipment manuals and software diskettes. Open all shipping containers upon receipt from the carrier and inspect the contents for shipping damage. Any indication of damage must be noted by both the recipient and the carrier. All claims for damage should be promptly filed with the carrier's representative.

Equipment received should be checked against the packing list to ensure that both the proper quantity and type of equipment was shipped. Serial numbers must be verified. The ID plates are located on the rear of the microcomputer and diskette drive modules. Figure 3-1 shows a breakdown of the diskette label information. The MICROSYSTEM 6600 provides for several power options. Check customer purchase order or packing slip to determine the power option provided with a particular unit.

If the MICROSYSTEM 6600 is not to be installed immediately on receipt, the equipment should be returned to the shipping containers for storage. Equipment should be stored in a cool, dry location. Special care must be taken with the package containing the software diskettes and manuals. The diskettes must not be exposed to extremes in temperature or humidity, contaminated by foreign material, or exposed to strong magnetic or electrical fields.

Any returns to the factory must be packed in either the original container or a substitute container of equal strength and durability. The original packing material or a substitute at least 2 inches thick should be provided on all sides of the equipment. Each module must be packaged separately. Any loose items such as cables, etc., used with the returned item must be shipped. A description of the defect, the cause of the defect (if known) and the name and address of the sender must accompany any returned equipment.

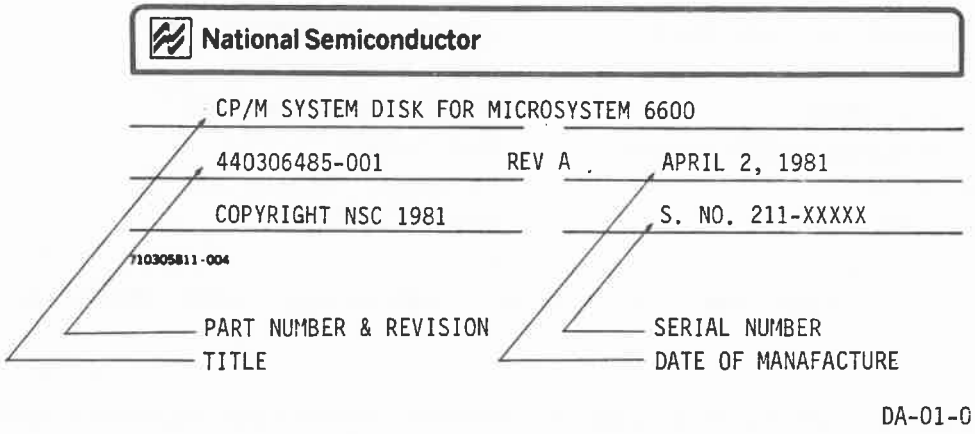


Figure 3-1 Diskette Label Information

Returned equipment is to be sent to the following address:

Microcomputer Service Center
675 Almanor Avenue
Sunnyvale, California 94086
Attn: Microcomputer Service Manager Ref: SRA#_____
Mail Stop: 15236
Telephone: (408) 737-6270

Address correspondence to the following facility:

Domestic Contact:	European Contact:
National Semiconductor Corporation	National Semiconductor GmbH
2900 Semiconductor Drive	Industriestrasse #10
Santa Clara, CA 95051	D8080 Fuerstenfeldbruck
Attn: Microcomputer Service Manager	West Germany
Mail Stop: 15236	Telephone: (08141) 1371
Telephone: (408) 737-6270	Telex: 05-27649

In other countries, contact your local National Semiconductor Sales Office or Authorized Representative.

NOTE: Do not return any material to National Semiconductor without first obtaining a Service Return Authorization Number (SRA#). To obtain an SRA#, call the telephone number listed above.

3.4 PREINSTALLATION INSPECTION

The delivered equipment must be inspected prior to installation to ensure all items are complete, there is no apparent damage, and that specified customer options have been provided.

Each equipment module is provided with an ID label that lists the equipment serial number, power configuration, and fuse requirements. These labels are located on the rear of the MICROSYSTEM 6600 modules Check the power requirements listed on the equipment labels to ensure they match the available on-site power.

3.4.1 Microcomputer Module Inspection

Remove the rear panel from the microcomputer module and inspect the card cage to ensure that all BLC boards are properly inserted. Figure 3-2 shows the location of the three standard boards. Check that all board edge connectors are properly inserted. Replace the rear panel.

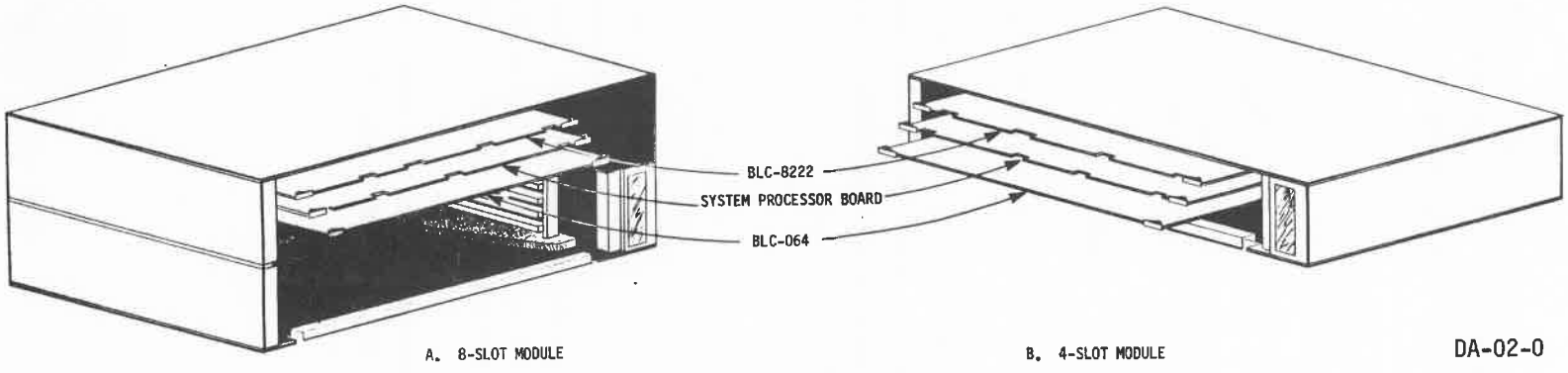


Figure 3-2 Location of Standard Boards

3.4.2 Diskette Drive Module Inspection

Inspect each diskette drive to ensure all packing material is removed from the diskette slots. The module has two slots that receive the diskettes. It is necessary to open the disk slot access doors and remove the packing material before installing the diskette drive module.

3.5 INSTALLATION AND CABLING

Installation of the modules should be completed following electronic's industry standards for installing rack-mount equipment. As the location and orientation of the modules varies from site to site, no detailed installation procedures are included in this manual.

CAUTION

Before plugging in the AC power cords, ensure BOTH disk drives are empty.

Figure 3-3 shows the location of the connectors for the 50-conductor ribbon cable that connects the microcomputer and diskette drive modules. Once the modules are mounted, this cable should be installed. The connectors are non-symmetric; if resistance is encountered in installation, check that the connectors are properly matched.

3.6 PERIPHERIAL INSTALLATION

The MICROSYSTEM 6600 is shipped equipped to interface with a Centronics printer and a CRT Terminal. The rear panel of the microcomputer module has a 36-pin connector for the printer and a 25-pin connector for the terminal. Figure 3-4 shows the location of these connectors. Details of the pin assignments for these connectors are given in Chapter 4 of this manual. Installation of peripherial equipment requires only the insertion of the cable in the proper connector.

NOTE: There is a wide varity of peripheral equipment that might be used with the MICROSYSTEM 6600. Questions regarding suitability and installation should be directed to a National Semiconductor Field Applications Engineer.

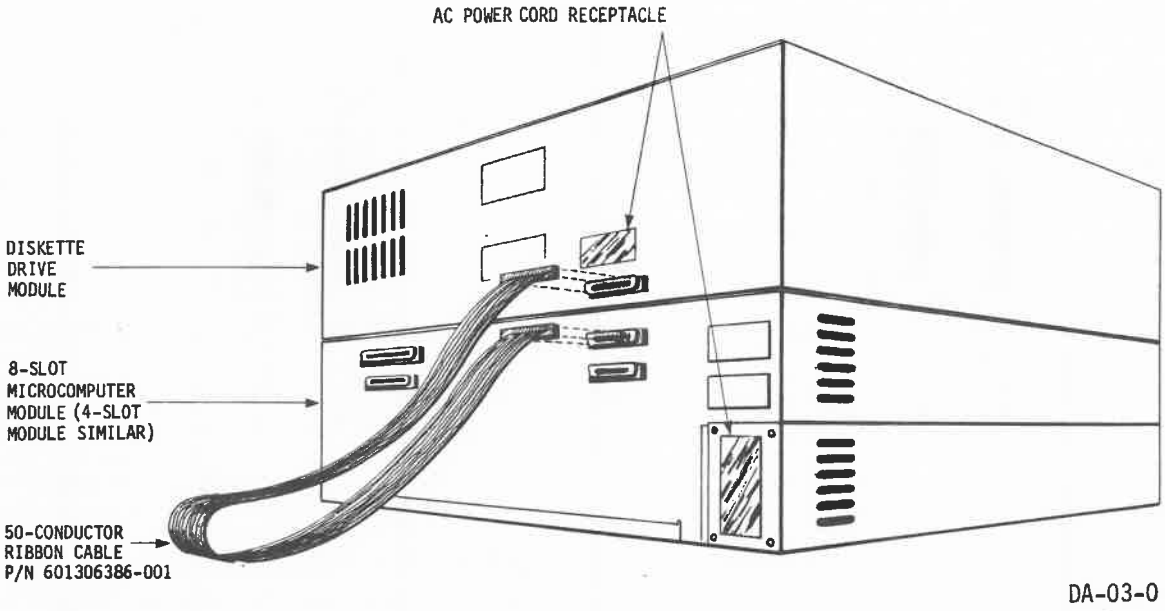
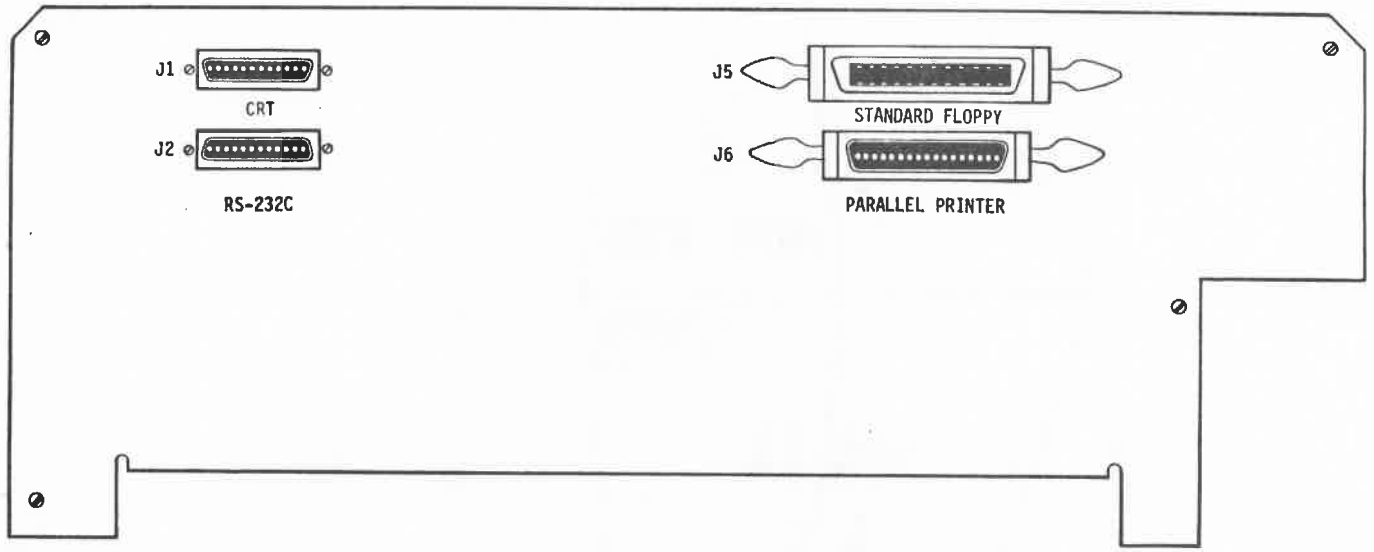
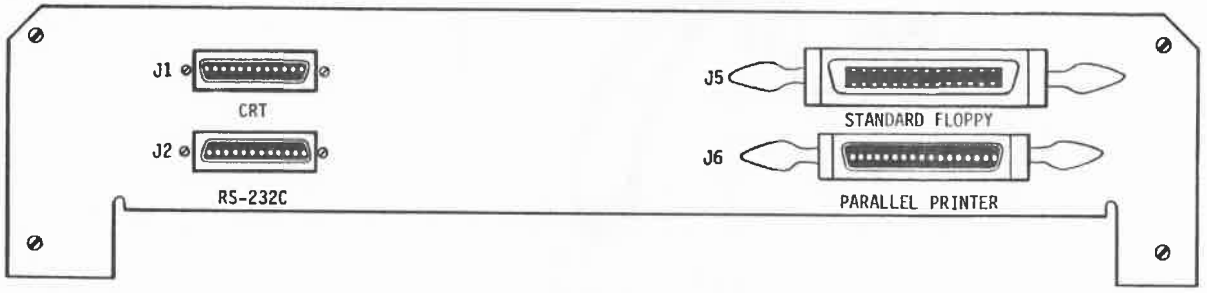


Figure 3-3 Installing the Interface Cable



A. 8-SLOT MODULE



B. 4-SLOT MODULE

DA-04-0

Figure 3-4 Rear Bulkhead Showing Standard Connectors

3.7 CONTROLS AND INDICATORS

3.7.1 Microcomputer Module

Figure 3-5 shows the location of the controls and indicators on the microcomputer module. As shown, there is a lighted Power ON/OFF switch and a RESET switch. The power switch controls AC power to the cooling fans and DC power supply. The RESET switch, when pressed, activates the backplane signal INIT/, which causes the CPU to restart operation.

3.7.2 Diskette Drive Module

Figure 3-6 shows the location of the controls and indicators on the diskette drive module. As shown, there is a lighted Power ON/OFF switch and two drive select lamps, one for each drive. The power switch controls AC power to the drive power supply, the disk drives, and the cooling fan. The drive select lamps light when the particular drive is selected for a read, write, or seek operation. The drive access door must not be opened when the select lamp on the drive is lit, or damage to the disk may occur.

3.8 OPERATIONAL CHECKS

Once the MICROSYSTEM 6600 modules are installed and cabled together, and any peripherial equipment is installed and connected to the system, the system operation should be checked using the diagnostic software provided with the system. This subsection includes instructions for turning on the system, loading the diagnostic software diskette, and running the diagnostic routines. The diagnostics provide a thorough check of the system; failure of any test indicates a problem which should be resolved by following the maintenance procedures in Chapter 8 of this manual.

NOTE: Use of the diagnostic software requires a terminal device be connected to the MICROSYSTEM 6600.

3.8.1 System Power-Up

To power-up the MICROSYSTEM 6600, complete the following steps:

1. Ensure BOTH disk drives are empty.

2. Plug both AC power cords into suitable outlets.

3. Set both power switches to the ON position. The switches should light and the fans should come on. If not, refer to Chapter 8, SYSTEM MAINTENANCE.

4. Following manufacturer's procedures, power-up any peripheral equipment connected to the system.

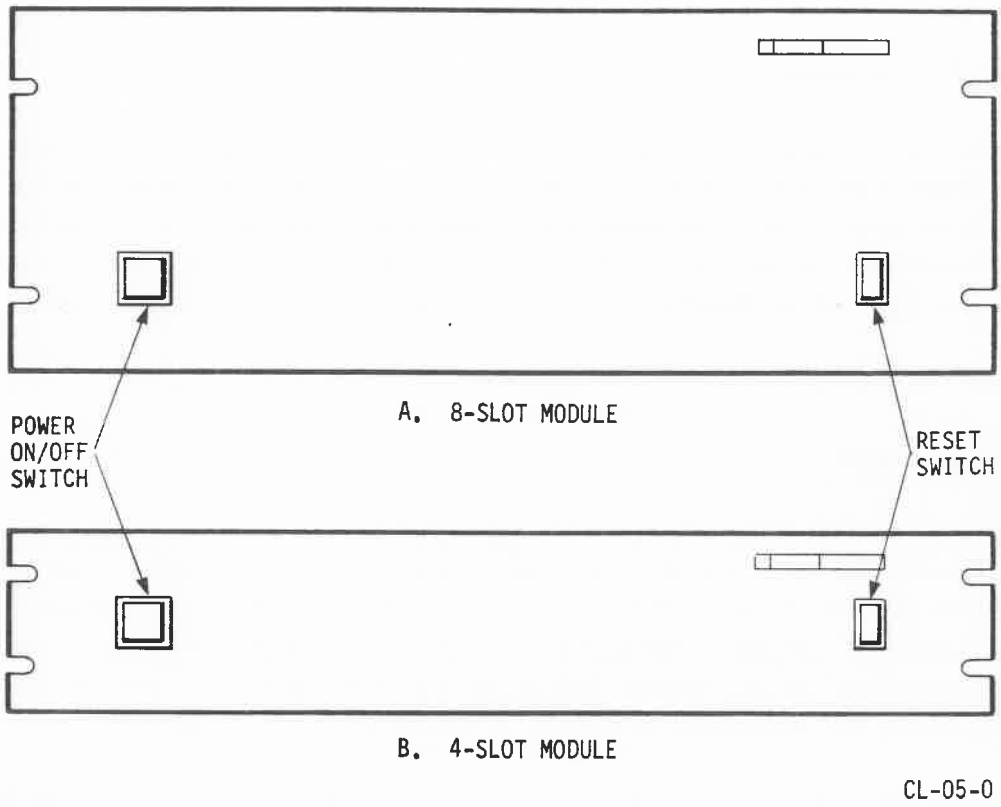


Figure 3-5 Location of Microcomputer Module Controls and Indicators

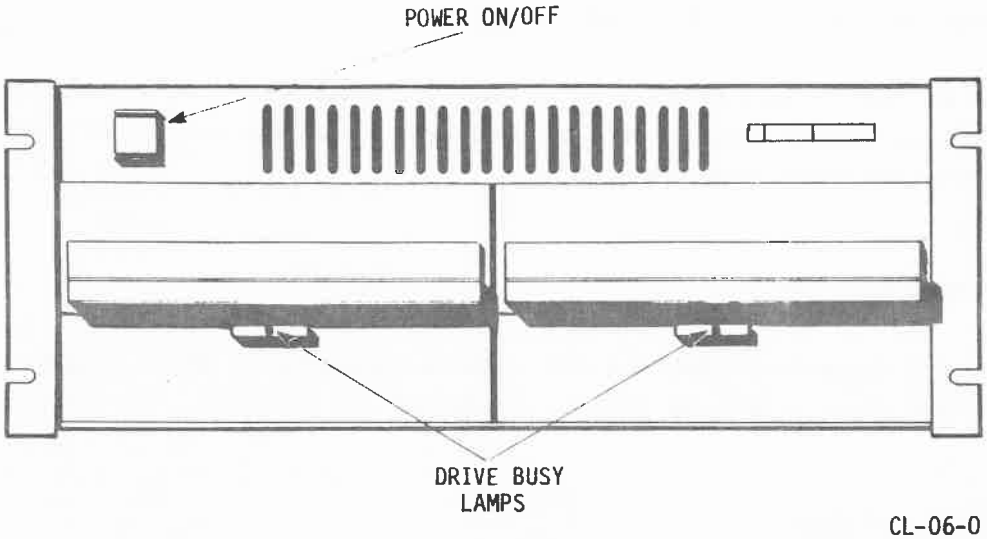


Figure 3-6 Diskette Drive Module Controls and Indicators

3.8.2 Loading The Diagnostic Diskette

The diagnostic software is loaded via the boot PROM on the System Processor board and the bootstrap loader resident on the disk. To load the diagnostic software, proceed as follows:

a. Insert the diagnostic software diskette in drive A (the left-hand drive). See Figure 3-7 for the correct method of inserting the diskette.

b. Momentarily press the RESET switch on the microcomputer module.

c. At the terminal, repeatedly press the RETURN key until either an error message or the menu shown in Figure 3-8 is displayed.

d. If the boot firmware should detect a fault that makes loading impossible, one of the error messages shown in Table 3-1 will be displayed. Should this occur, take the suggested action and repeat Steps a through c.

3.8.3 Load Error Procedure

If a disk error is detected by either the PROM resident diagnostics or loader program, an attempt is made to print that error to both the terminal and printer (if available). The error printout is as follows:

```
XXXXXX.XXX load error
where XXXXXX.XXX is either 6600.DM or Geography
```

Should a disk error be encountered, complete the following:

a. Remove the diagnostic diskette from the drive used when the error occured.

b. Insert the diskette in the other drive.

c. Press the RESET switch on the microcomputer module.

d. The menu shown in Figure 3-8 should be displayed on the terminal. If not, refer to Chapter 8.

3.8.4 Normal Diagnostic Operating Procedures

The purpose of the normal operating procedures is to run all the required subtests on all the equipment so that the hardware is 100% tested. The normal operating procedures should be used during installation. These procedures are explained in the following paragraphs.

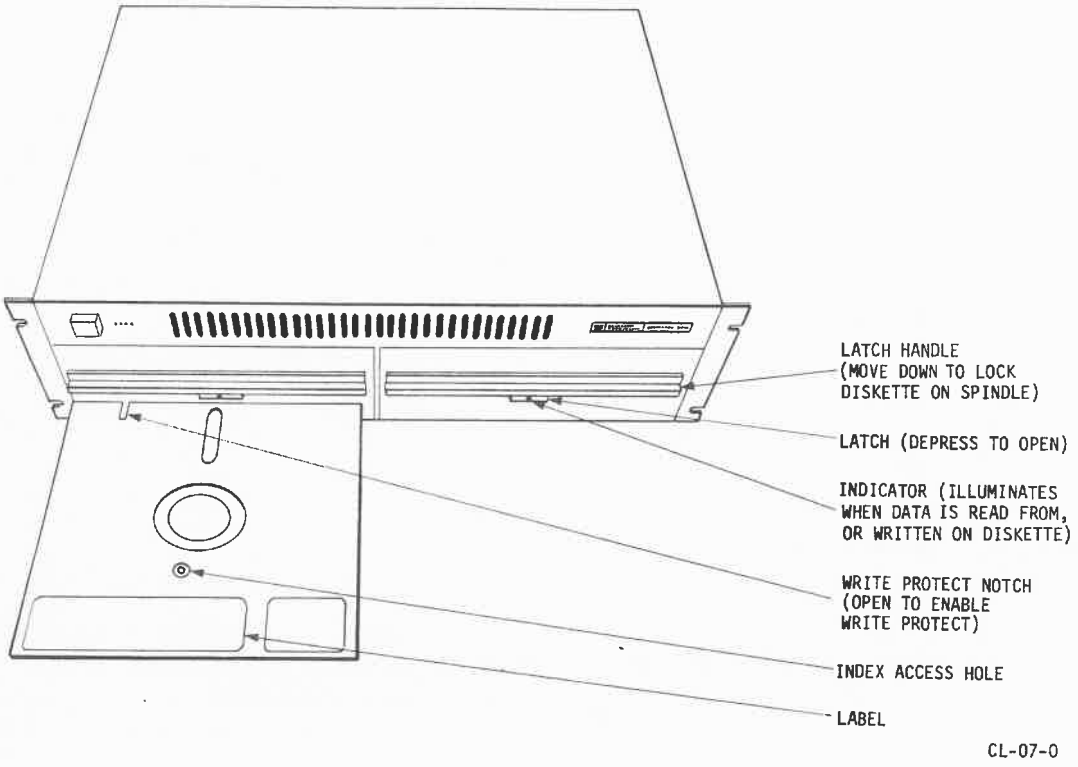


Figure 3-7 Inserting the Diagnostic Diskette

```
Z6600 Diagnostic Monitor    Version n.n    mm/dd/yy

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Command         Parameter         Comment

DE              ALL/CRT/LPT       Select listing devices

ME              ALL/ERROR         Select type of message

OP              ---               Display options selected

RE              O/N               Repeat infinitely/n times

RU              ---               RUN

SU              AU/N/ALL          Select subtest

TE              ALL/XXXXXX        Select test

Enter commands
>
```

NOTE: If any of the above items do not appear on the menu, it is not yet implemented, but will be in future revisions.

Figure 3-8 Diagnostic Software Menu

TABLE 3-1 BOOT PROM ERROR NUMBERS AND SUGGESTED ACTIONS

MESSAGE	EXPLANATION	SUGGESTED ACTION
No response	Basic CPU Problem	Check power supply, system clock, Replace System Processor board.
Long delay	Acknowledge from memory board is not received	Replace RAM board (BLC-064).
Error 00	Checksum failure	Replace Boot Firmware PROM.
Error 01	Instruction or Register failure	Replace System Processor board.
Error 10	System memory Read/ Write error	Replace RAM board (BLC-064).
Error 11 or Error 12	System memory failure Monitor result not Guaranteed	Replace RAM board (BLC-064).
Error 20	Processor board parallel I/O error	Replace System Processor board.
Error 21	Interval Timer error	Replace System Processor board.
Error 22	Interrupt Controller error	Replace System Processor board.
Error 30	No response from Floppy Disk Controller	Replace Flexible Disk Controller (BLC-8222).
Error 31	Floppy Disk Controller Checksum test failed	Replace Flexible Disk Controller (BLC-8222).
Error 32	Floppy Disk Controller on-board RAM failed	Replace Flexible Disk Controller (BLC-8222).
Error 33	INS1791 Floppy Controller chip failed	Replace Flexible Disk Controller (BLC-8222).
Error 40	PROM off failed	Replace System Processor board.

To initiate the normal procedures, enter the following after the "Enter commands" message is displayed:

>RU (CR)

NOTE: In this and all remaining examples, required operator inputs are underlined and (CR) means press the carriage return key on the terminal.

After the RU command is entered, the first device test program is loaded into RAM memory and the following message is displayed:

XXXXXX Version n.n mm/dd/yy loaded
where: XXXXXX is the test program name

When the first test program is complete, the next test program is loaded. This process repeats until all the required tests are completed. As each subtest is run within a test program, all messages are displayed on both the terminal and printer, if available. At the end of each subtest, a message is displayed indicating whether the test passed or not. For those subtests that require a visual check, as for the printer, the display reads EXITED rather than PASSED.

When all tests are complete, the "Enter commands" message is displayed.

Table 3-2 lists the device test programs in the order they are run during normal operating procedures. Figure 3-9 shows a typical display resulting from normal operating procedures where no errors are encountered. If errors should be encountered, refer to Chapter 8.

NOTE: This command initiates the running of all automatic subtests only. Manual and utility subtests can be initiated as described in the procedures in Chapter 8. If no printer is attached to the system the automatic printer subtests will respond with the appropriate error messages.

3.8.5 Optional Operating Procedures

Optional operating procedures allow the user to select a particular device test, a subtest in a given device test, error messages, output device, or to run and/or repeat tests. These procedures are typically used during maintenance, as opposed to installation checks, and are described in Chapter 8.

3.8.6 Error Messages

Table 3-3 lists the error messages that might be encountered using the diagnostic software. Handling of diagnostic errors is covered in Chapter 8.

TABLE 3-2 ORDER OF THE DIAGNOSTIC TESTS

TEST NAME	DESCRIPTION	EXECUTION SEQUENCE
CPU	Processor Test	1
MEMT1	Memory Test Part 1	2
MEMT2	Memory Test Part 2	3
CRT	CRT Test	4
CENPTR	Centronics Printer Test	5
FLOPPY	Flexible Disk Test	6
SERIAL	RS232C Serial Port Test	7

Execution sequence is the order in which device test programs are loaded and run under the normal loading procedure.

```
Z6600 Diagnostic Monitor Version n.n    mm/dd/yy

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All Rights Reserved

Command         Parameter           Comment

DE              ALL/CRT/LPT         Select listing devices
ME              ALL/ERROR           Select type of message
OP              ---                 Display options selected
RE              O/N                 Repeat infinitely/n times
RU              ---                 Run
SU              AU/N/ALL            Select subtest
TE              ALL/XXXXXX          Select test

Enter commands
>RU (cr)
CPU             Version n.n     mm/dd/yy        loaded
CPU             subtest 001     passed
     .
     .
     .
MEMT1           Version n.n     mm/dd/yy        loaded
MEMT1           subtest 001     passed
     .
     .
(refer to each test program specification for details)
     .
     .
Command         Parameter           Comment

DE              ALL/CRT/LPT         Select listing devices
ME              ALL/ERROR           Select type of message
OP              ---                 Display options selected
RE              O/N                 Repeat infinitely/n times
RU              ---                 Run
SU              AU/N/ALL            Select subtest
TE              ALL/XXXXXX          Select test

Enter commands
>
```

Note: 1. The operator input is underlined.

Figure 3-9 Sample Printout Of Normal Operating Procedure

TABLE 3-3 DIAGNOSTIC ERROR MESSAGES

MESSAGE	MEANING
Checksum error (XXH) found	A load error occurred during the loading of test program. XX is the checksum value in hexadecimal.
XXXXXX - file not found	A non-existent test program was requested. XXXXXX is the filename.
DM memory error at XXXX: expected YY is ZZ	Diagnostic memory test detected an error in the 16K of RAM reserved for test programs. XXX = memory address where error was detected YY = expected hexadecimal pattern ZZ = current content of location XXXX
Invalid entry	A syntax error was detected in the keyboard command. This error is cleared by entering the correct command format.
CRT error	A hardware error was detected by the diagnostic software during testing of the CRT terminal.
Disk error	A hardware error was detected by the diagnostic software during testing of the disk drive.
Printer error	A hardware error was detected by the diagnostic software during testing of the printer.
Invalid subtest selected | Enter commands >	The subtest number exceeds the maximum number of subtests specified in the particular test software loaded in RAM. To clear this error, reenter the correct subtest number.
XXXXXX. subtest nn error mm	This is an error message from a test program XXXXXX. = the test program name nn = the subtest number mm = the error identification code. Refer to the individual test program description given in Chapter 8 for error identification code lists.

Chapter 4

HARDWARE DESCRIPTION

4.1 GENERAL INFORMATION

This chapter provides a physical and functional description of the hardware provided with the MICROSYSTEM 6600.

The system consists of two rack-mountable electronic assemblies which are connected together with a 50-conductor ribbon signal cable. One assembly consists of a card cage with logic boards (microcomputer module); the other assembly consists of two 8-inch standard size flexible disk drives (diskette drive module). The system is offered in two basic configurations: one configuration consists of a 4-slot microcomputer module with the diskette drive module, and the other configuration consists of an 8-slot microcomputer module with the diskette drive module.

The remainder of this chapter is in five parts. A description of the physical locations of subassemblies within each module, functional description of the MICROSYSTEM 6600 architecture, a functional description of the microcomputer module components, a functional description of the flexible disk drive module components, and an operational description of the boot loader firmware supplied with the system.

4.2 LOCATION OF COMPONENTS

Figure 4-1 is a line drawing of the 4-slot microcomputer module showing the location of field-replaceable components. Figure 4-2 is a line drawing of the 8-slot microcomputer module showing the location of field-replaceable components. Figure 4-3 is a line drawing of the diskette drive module, showing the location of major components. The diskette drive module is considered a functional unit; field replacement of subassemblies within this module is not recommended.

4.3 SYSTEM ARCHITECTURE

The architecture of the MICROSYSTEM 6600 is based on the Intel Corporation MULTIBUS specification. The MULTIBUS interface is a flexible bus structure that allows system components to interact with each other. Memory and I/O data transfer, direct memory accesses, interrupt generation and handling, etc., are all supported by the bus structure.

The bus supports direct addressing of up to 1M byte of system memory via a 20-bit address bus. Either 8- or 16-bit data transfers can be made. A master-slave handshake and provision for multiple bus masters allow for both sharing of control functions and a fast data throughput.

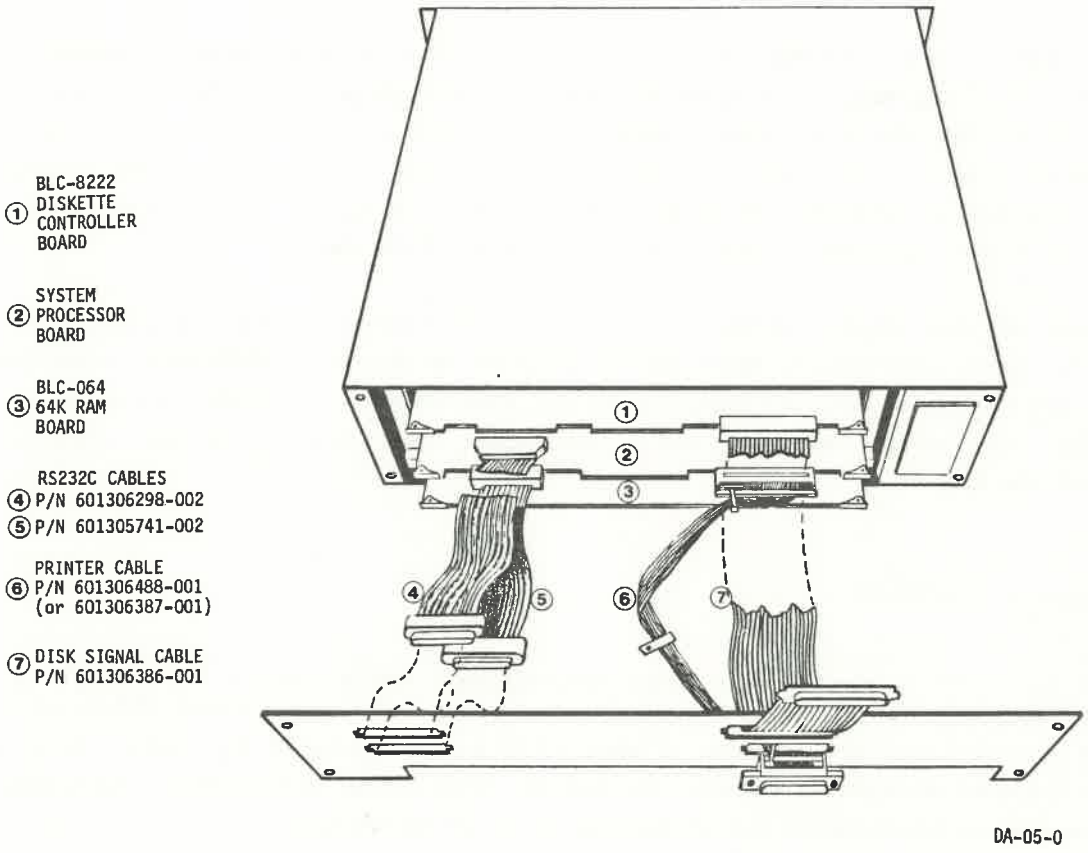


Figure 4-1 4-Slot Microcomputer Module - Location of Field Replaceable Components

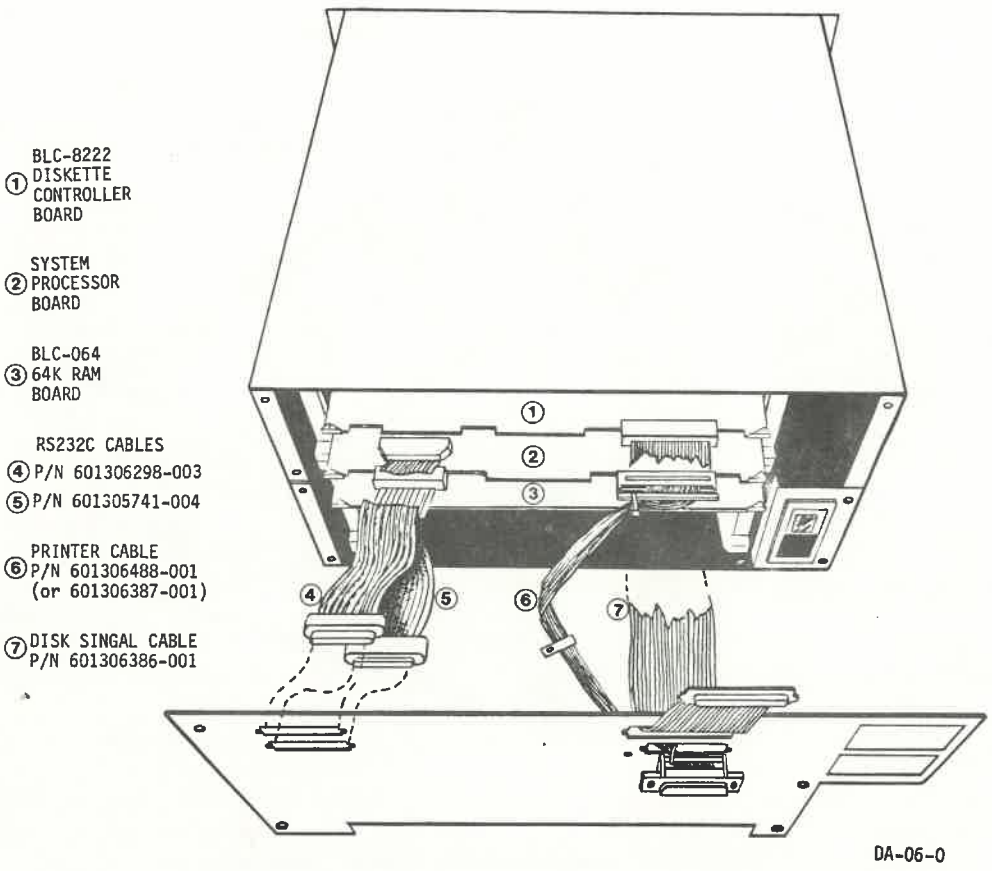

① BLC-8222 DISKETTE CONTROLLER BOARD
② SYSTEM PROCESSOR BOARD
③ BLC-064 64K RAM BOARD
RS232C CABLES
④ P/N 601306298-003
⑤ P/N 601305741-004
⑥ PRINTER CABLE P/N 601306488-001 (or 601306387-001)
⑦ DISK SINGAL CABLE P/N 601306386-001
DA-06-0

Figure 4-2 8-Slot Microcomputer Module - Location of Field Replaceable Components

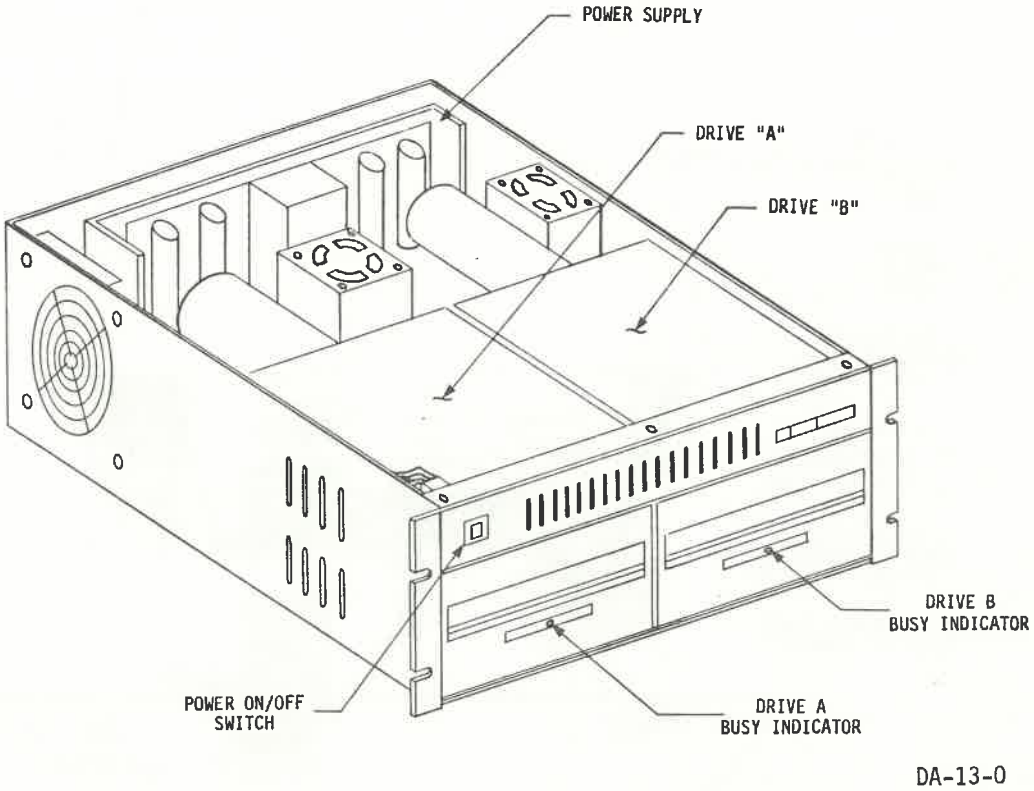


Figure 4-3 Diskette Drive Module Components

The MICROSYSTEM 6600 supports all the MULTIBUS signals defined in the MULTIBUS specification. Table 4-1 lists the P1 MULTIBUS board connector signal assignments and Table 4-2 lists the P2 auxiliary connector assignment of optional bus signals.

4.3.1 CPU Architecture

The Z80A based System Processor Board features software-programmable interrupt controllers and timers, one socket for 2K x 8-bit ROM/PROM's, two Serial I/O Interfaces, two programmable Parallel I/O Interfaces providing 48 signal lines for transfer and control of data to or from peripherals, and a System Bus Controller for interfacing the board with other bus masters, such as CPU and Direct Memory Access devices. A more complete description of the board is provided in Section 4.4.4.

4.3.2 Bus Masters

Two Bus Masters are provided within the system: the Flexible Disk Controller and the CPU Board. The bus priority scheme provided within the system is serial, passing from the Flexible Disk Controller to the CPU Board and through the RAM Board to the spare card slot(s). The start of the serial chain is provided by a GROUND wire on pin 15 (BPRN/) of the P1 connector of card slot 1. Since a maximum total of six serial bus masters can be configured with SERIES/80 MULTIBUS boards, the user can add a maximum of four additional masters if the appropriate number of card slots are available in the microcomputer module.

4.3.3 Reset

The RESET circuitry within the system consists of: a DPDT switch located on the front panel, debounce circuitry located on the RESET PWB, and wiring to the card cage backplane. When the RESET switch is depressed, the output of the debounce circuit remains low, grounding the backplane signal INIT/ located on pin 14 of the P1 connector. Figure 4-4 shows the debounce circuitry that interfaces the RESET switch to the card cage backplane.

4.3.4 Memory

The memory within the system consists of 64K bytes of dynamic RAM located on the BLC-064 memory board, and 2K of PROM located on the System Processor board. The dynamic RAM is located on the system MULTIBUS and therefore is accessible by both system bus masters. The 2K of PROM is located on the CPU microbus and therefore is only accessible by the on-board Z80A microprocessor. The PROM is located starting at location zero and shadows RAM which can only be accessed by using the I/O mapped ROM/RAM-OFF capability. The PROM is composed of one 2716 (2K byte) socket location and contains the boot loader firmware program.

TABLE 4-1 PIN ASSIGNMENT OF BUS SIGNALS ON MULTIBUS BOARD CONNECTOR (P1)

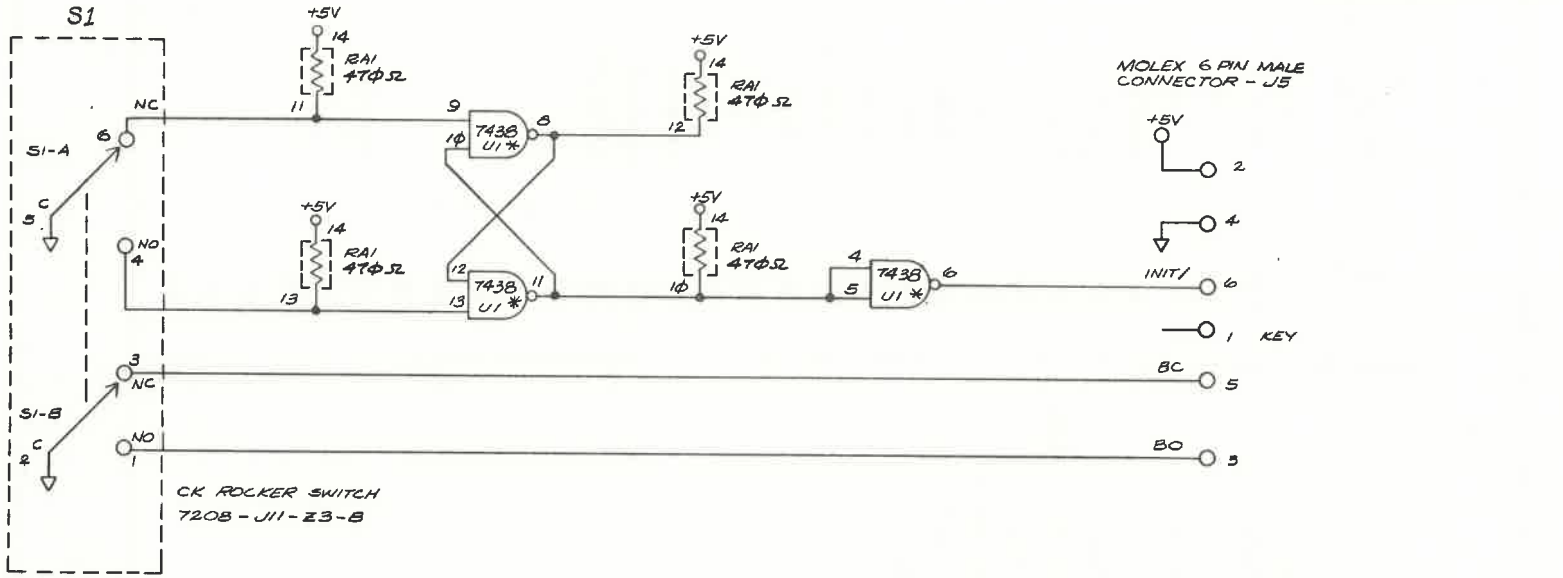
	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	-5V	-5Vdc	10	-5V	-5Vdc
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/	Bus Clock	14	INIT/	Initialize
	15	BPRN/	Bus Pri. In	16	BPRO/	Bus Pri. Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 disable RAM
	25		Reserved	26	INH2/	Inhibit 2 disable PROM
BUS CONTROLS AND ADDRESS	27	BHEN/	Byte High Enable	28	AD10/	
	29	CBRQ/	Command Bus Request	30	AD11/	Address
	31	CCLK/	Constant Clk	32	AD12/	Bus
	33	INTA/	Intr Acknowledge	34	AD13/	
INTERRUPT	35	INT6/	Parallel	36	INT7/	Parallel
	37	INT4/	Interrupt	38	INT5/	Interrupt
	39	INT2/	Requests	40	INT3/	Requests
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address	50	ADR9/	Address
	51	ADR6/	Bus	52	ADR7/	Bus
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/	Data	66	DAT9/	Data
	67	DAT6/	Bus	68	DAT7/	Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

TABLE 4-2 P2 CONNECTOR PIN ASSIGNMENT OF OPTIONAL BUS SIGNALS

(COMPONENT SIDE)			(CIRCUIT SIDE)		
PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	GND	Signal GND	2	GND	Signal GND
3	5VB	+ 5V Battery	4	GVB	+ 5V Battery
5		Reserved	6	VCCPP	+ 5V Pulsed Power
7	-5VB	- 5V Battery	8	-5VB	- 5V Battery
9		Reserved	10	Reserved	
11	12VB	+12V Battery	12	12VB	+12V Battery
13	PFSR/	Power Fail Sense Reset	14	Reserved	
15	-12VB	-12V Battery	16	-12VB	-12V Battery
17	PFSN/	Power Fail Sense	18	ACLO	AC Low
19	PFIN/	Power Fail Interrupt	20	MPRO/	Memory Protect
21	GND	Signal GND	22	GND	Signal GND
23	+15V	+15V	24	+15V	+15V
25	-15V	-15V	26	-15V	-15V
27	PAR1/	Parity 1	28	HALT/	Bus Master HALT
29	PAR2/	Parity 2	30	WAIT/	Bus Master WAIT STATE
31			32	ALE	Bus Master ALE
33			34	Reserved	
35			36	Reserved	
37			38	AUX RESET/	Reset Switch
39			40		
41			42		
43			44		
45	Reserved		46		
47			48		
49			50	Reserved	
51			52		
53			54		
55			56		
57			58		
59			60		

Notes:

1. PFIN/, on slave modules, if possible, should have the option of connecting to INT0/ on P1.
2. All undefined pins are reserved for future use.



SPARE GATES			
CMP TYPE	LOCATION	OUT PIN	QTY
7438	U1	3	1
	RA1	1,2,3,4,5,6,7,8,9	9

Figure 4-4 MSC-6600 Rack-Mount Computer Module Reset Logic Diagram

4.3.5 I/O Devices

The system I/O devices are listed below:

- 48 Parallel Lines
- Two RS232C Interfaces
  Three Programmable Timers
- Memory Map
- System Control Bits
- BLC-8222 Flexible Disk Controller

With the exception of the Flexible Disk Controller, all I/O devices are physically located on the System Processor board and are addressable only by the on-board Z80A processor. The majority of I/O functions are provided by LSI devices and are configured to support existing system devices such as the printer and CRT interfaces. The specific devices, address, and bit assignments within the devices are listed in Table 5-3 in Chapter 5.

4.3.6 Interrupts

A total of fifteen interrupt levels are provided within the system. The interrupt signals are wired to inputs on the two 8259 interrupt controllers located on the System Processor board. The device interrupt assignments are as follows:

System Processor Board

0 RS232 #1 RRDY (Receiver Ready)
1 RS232 #2 RRDY (Receiver Ready)
2 Interval Timer (8253)
3 Backplane Interrupt Controller (Slave 8259)
4 RS232 #1 TRDY (Transmitter Ready)
5 RS232 #2 TRDY (Transmitter Ready)
6 Printer Not Busy (8255)
7 Unassigned Parallel Port (8255)

Backplane

0-4 Unassigned
5 Floppy Disk Controller - Not Busy
6-7 Unassigned

4.4 MICROCOMPUTER MODULE EQUIPMENT DESCRIPTION

4.4.1 Physical Description

The two (4/8 slot) microcomputer modules consist of 19 inch rack mountable electronic assemblies which are constructed of the following items:

- Sheet Metal Enclosure Parts
- DC Power Supply
- Two AC fans
- AC/DC Internal Power Harness
- Card Cage(s)
- Reset Logic Board
- Three MULTIBUS Logic Boards
  - BLC-8222 FM/MFM Flexible Disk Controller
  - System Processor Board
  - BLC-064 RAM Board
- Four Internal Signal Cables
  - Disk Signal Cable
  - Printer Signal Cable
  - Two RS232C Signal Cables

The two modules differ in the following specific areas (MSC-6601 vs MSC-6605):

- Physical Height (3.5 in. vs 7.0 in.)
- Weight (37 lbs. vs 49 lbs.)
- Card Cages (One vs Two)
- Total Card Slots (Four vs Eight)
- Available Unused Card Slots (One vs Five)
- DC Power Supply Capability
- Fan Size

AC Power. AC input power is provided to the module through an external power cord which is plugged into a power receptacle provided at the rear of the module. A lighted ON/OFF switch is provided on the module front panel along with a RESET switch. A fuse receptacle and a factory set voltage selector are provided on the rear of the module at the power receptacle connection. Three panel mount connectors are provided on the module back for connection to the system peripherals. A 50-pin connector is provided for connection to the system disk module, a 36-pin connector is provided for connection to a Centronics printer, and two 25-pin connectors are provided for connection to a CRT Terminal and the spare RS232C interface.

Within the module, AC power is wired to: the input fuse, line filter, ON/OFF switch, fans, and DC power supply input. The four DC voltage outputs from the power supply (+5V, -5V, +12V, -12V) provide power to the card cage(S). The +5 volt output is also used to power logic on the reset board.

Board Configuration. The board configuration within the module is listed below. Slot 1 is physically the top slot.

Slot	Board
1	BLC-8222 FM/MFM Disk Controller
2	System Processor Board
3	BLC-064 RAM Board
4	Spare
5	Spare for Eight Slot Module
6	Spare for Eight Slot Module
7	Spare for Eight Slot Module
8	Spare for Eight Slot Module

Internal Cabling. Four internal cables provide connections between the logic boards and the system external peripherals. The cabling between the boards and the rear panel connections is listed in Table 4-3.

I/O Connectors. Three of the four panel mount connectors provide connections to the three external system devices (diskette drive module, Centronics Printer, CRT terminal). The connector and signal pin assignment for the disk interface is given in Section 4.5 and the specifications on the other connector interfaces are listed in Tables 4-4 and 4-5.

4.4.2 Card Cage Arrangement

Both the 4-slot and 8-slot microcomputer modules use the BLC-604 card cage. In addition, the 8-slot module uses the BLC-614 expansion card cage. This equipment is described in the following paragraphs.

The BLC-604 is a 4-slot molded chassis and backplane. The backplane has a data, address and control signal bus, terminating networks; power supply connectors, and a bus extension circuit card edge connector.

In the 8-slot module, a four slot BLC-614 expansion card cage is plugged into the bus expansion connector on the BLC-604. Figure 4-5 shows a logic diagram of the BLC-604 card cage and Figure 4-6 shows the logic diagram of the BLC-614 card cage.

TABLE 4-3 INTERNAL CABLE CONNECTIONS

APPLICATION	CABLE P/N	BOARD CONNECTOR	PANEL CONNECTOR
Disk (4-slot) (8-slot)	601306409-001 601306409-002	BLC-8222 J2	J5
Printer (4- or 8-slot)	601306387-001	Sys. Pr. Bd. J1	J6
RS232C (4-slot) (8-slot)	601305741-002 601305741-004	Sys. Pr. Bd. J3	J1
RS232C (4-slot) (8-slot)	601306298-002 601306298-003	Sys. Pr. Bd. J4	J2

TABLE 4-4 CENTRONICS PRINTER INTERFACE

SIGNAL NAME	PIN	RETURN
BUSY	11	29
LIGHT DETECT	33	--
FAULT	32	--
PAPER EMPTY	12	--
SELECT	13	--
DATA 8	9	27
DATA 7	8	26
DATA 6	7	25
DATA 5	6	24
DATA 4	5	23
DATA 3	4	22
DATA 2	3	21
DATA 1	2	20
DATA STROBE	1	19
INPUT PRIME	31	30

Mating connector - Amphenol 36 pin
Connector P/N 57-50360 (standard equipment rack)
or
P/N 57-30360 (if equipment rack provides enough room)

TABLE 4-5 RS232C INTERFACES

SIGNAL NAME	PIN
PROTECTIVE GND	1
TRANS DATA	2
REC DATA	3
REQ TO SEND	4
CLR TO SEND	5
DATA SET RDY	6
SIGNAL GND	7
REC LINE SIG DET	8
-----	9
-----	10
-----	11
-----	12
SECONDARY CTS	13
-----	14
TRANS SIG ELE TIMING	15
SECONDARY REC DATA	16
REC SIG ELE TIMING	17
-----	18
SECONDARY RTS	19
DATA TERMINAL RDY/	20
-----	21
RING INDICATOR	22
-12V (FOR BLC-530)	23
+12V (FOR BLC-530)	24
+5V (FOR BLC-530)	25

Mating Connector - DB-25S Type

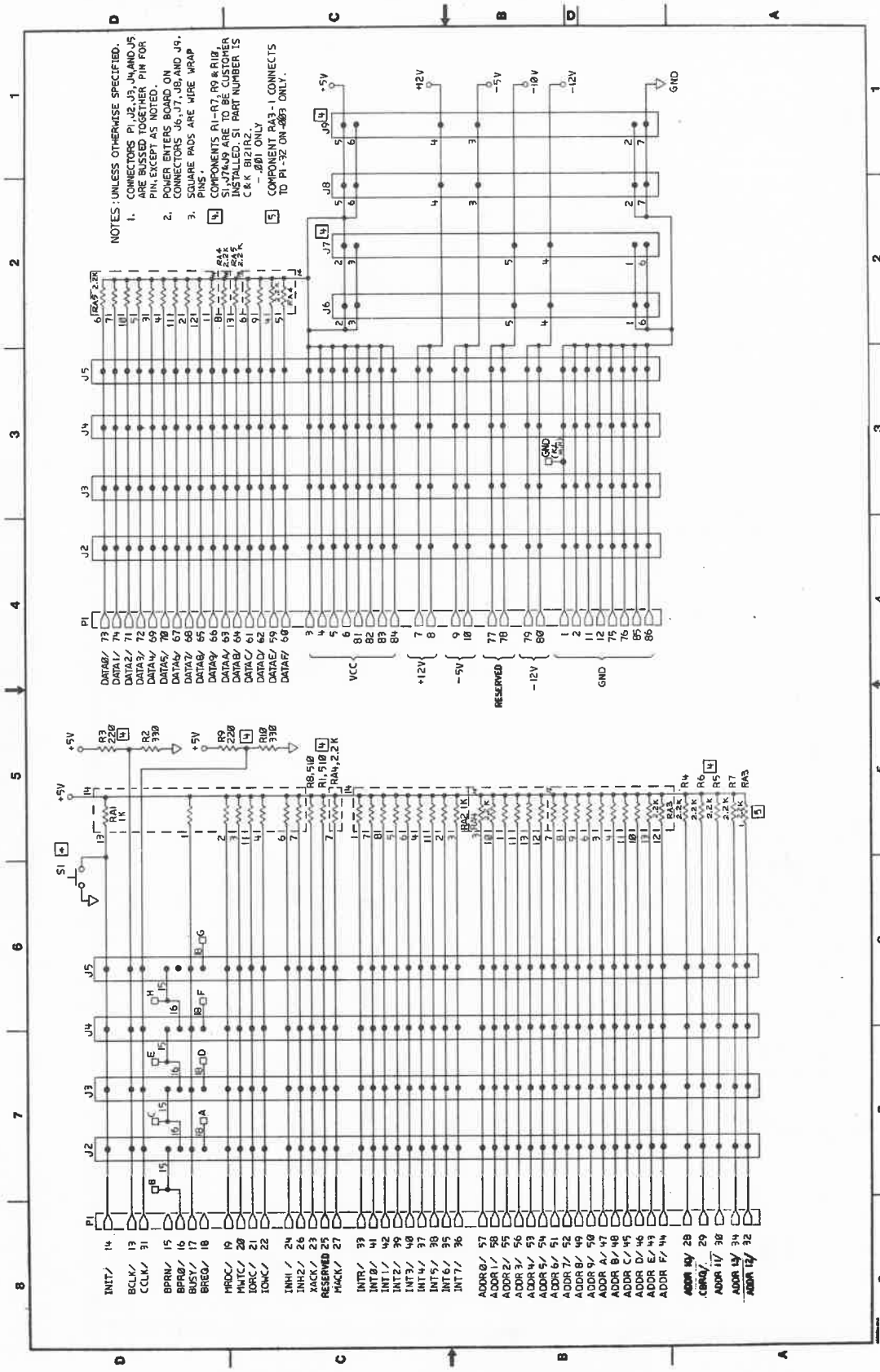


Figure 4-5 BIC-604 Backplane Logic Diagram

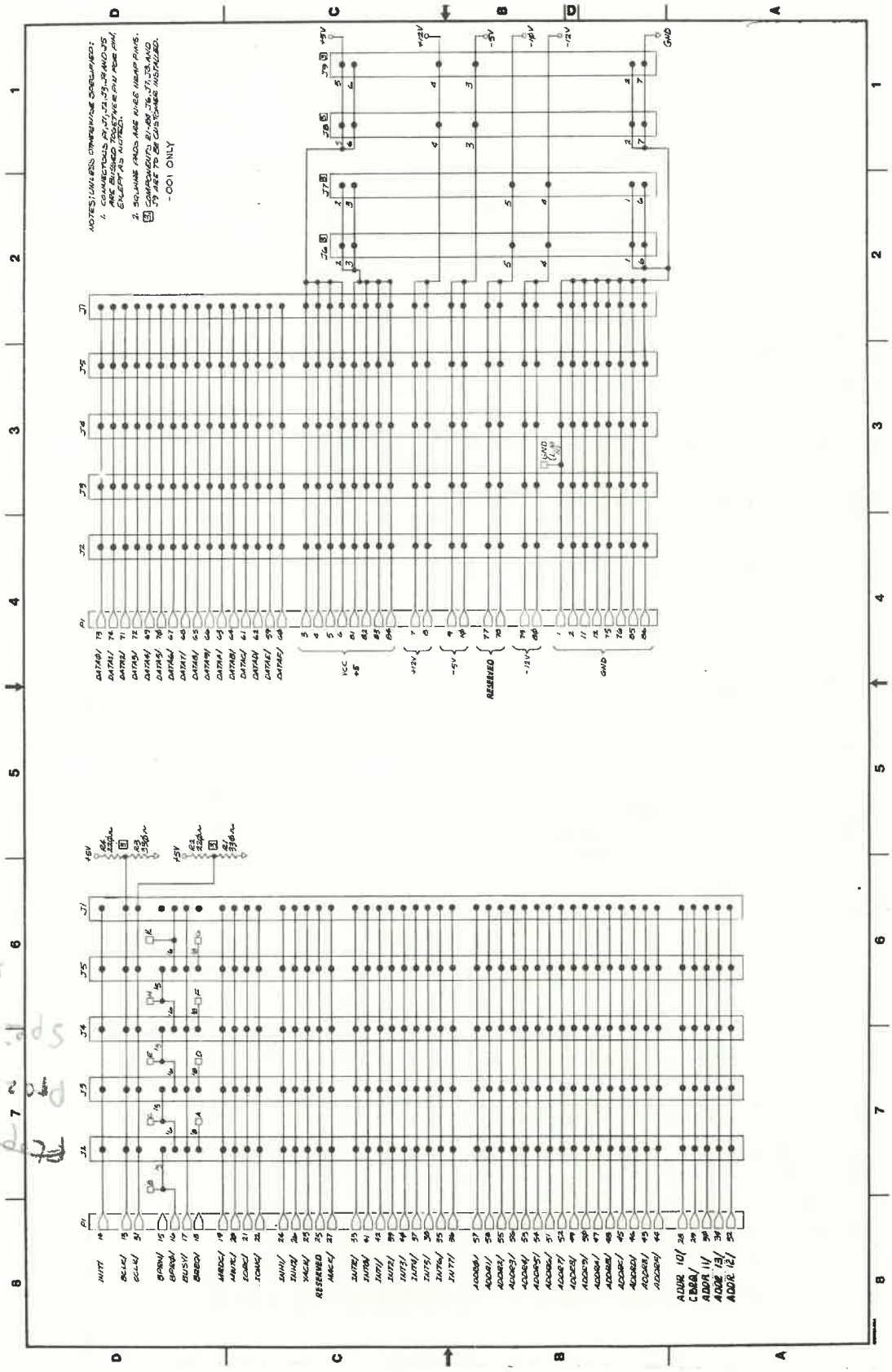


Figure 4-6 BLC-614 Backplane Logic Diagram

4.4.3 Power Supply Description

The 8-slot and 4-slot microcomputer modules have different power supplies. The 4-slot module is equipped with the BLC-635 power supply and the 8-slot module is equipped with the BLC-665 power supply. These units are described in the following paragraphs.

The BLC-635 and BLC-665 power supplies provide ±5 and ±12 volts of regulated DC power at maximum current over a temperature range of 0° to + 55°C. Table 4-6 summarizes the capacities of the power supplies.

The BLC-635 provides power for the CPU board, the BLC-064 RAM, and BLC-8222 Flexible Disk Controller with enough additional capacity to supply most configurations of one additional BLC-/SBC memory, I/O, or other expansion board, up to a total of 4 boards.

The BLC-665 supplies approximately twice the rated power of the BLC-635. The BLC-665 will power the standard system boards and most combinations of five additional expansion boards, up to a total of 8 boards.

Table 4-7 lists the available power used by the standard BLC boards, and the spare power available for both the 4-slot and 8-slot modules.

All outputs are current limited and have over-voltage protection. The AC input is fused for either 100-115 VAC or 200-230 VAC operation.

DC power is carried on cables keyed for compatibility to the BLC-604 System Card Cage.

4.4.4 System Processor Board Description

This section presents a general description of the System Processor board. For a more detailed description refer to Chapter 5 of this manual.

Physical Description

The System Processor is fabricated on a four-layer printed circuit board measuring 12 X 6-3/4 inches. The board plugs into the logic module card cage. It has six edge connectors which are configured as follows:

- P1 is the on-board MULTIBUS interface connector.
- P2 is reserved for production test points and other National BLC standard signals.
- J1 and J2 are the parallel I/O ports.
- J3 and J4 are the serial I/O ports which interface with RS232C communications.

TABLE 4-6 MICROCOMPUTER MODULE POWER SUPPLY CHARACTERISTICS

Output Current Rating

VDC	BLC-635	BLC-665
+5	14A	30A
-5	0.9A	1.75A
+12	2.0A	4.5A
-12	0.8A	1.75A

Current limit approximately 20% above rated values

Output Adjust Range

±5% minimum on all outputs around nominal voltage

Line Regulation

±0.1% on all outputs for 10% line change

Load Regulation

±0.1% on all outputs for 50% load change

Output Ripple and Noise

10mv peak-to-peak maximum on all outputs from DC to 500 KHz

Stability

±0.05% on all outputs for 8 hours at constant line, load, and temperature after 30 minutes of warm-up

Transient Response

±5% on all outputs maximum for less than 50 microseconds with 50% load change

Remote Sensing

Provided at P8 connector for +5 volts

Chassis Ground Insulation

All output returns isolated from chassis ground

Overvoltage Protection

Provided on all outputs and factory set to trip within the following range:

Output Voltage	OVP Trip Range
+5V	5.8V to 6.6V
-5V	-5.8V to -6.6V
+12V	14V to 16V
-12V	-14V to -16V

Overload and Short Circuit Protection

+5V -- Foldback current limiting with automatic recovery

-5V, +12V, -12V -- Current limited to extent no damage will occur for extended overload condition

TABLE 4-7 POWER USAGE IN FOUR- AND EIGHT-SLOT MODULES

	FOUR-SLOT				EIGHT-SLOT			
	+5VDC	-5VDC	+12VDC	-12VDC	+5VDC	-5VDC	+12VDC	-12VDC
Total Available	14A	0.9A	2.0A	0.8A	30A	1.75A	4.5A	1.75A
BLC-8222	1.75A	.01A	.075A	---	1.75A	.01A	.075A	---
Sys. Pr. Bd.	5.6A	.18A	.47A	.12A	5.6A	.18A	.47A	.12A
BLC-064	3.0A	.011A	.47A	---	3.0A	.011A	.47A	---
Spare Available	3.65A	0.7A	0.99A	.68A	19.7A	1.55A	3.49A	1.63A

Functional Description

The functional organization of the System Processor board is shown in the block diagram, Figure 4-7. The System Processor board contains the following major functional blocks:

- Processor
- Memory
- Programmable Interrupt Logic
- Input/Output
- Bus Interface

Processor

The Processor block contains a Z80A CPU, a Clock Generator, Address Buffers, Power-on Reset circuits, a Halt flip-flop, Ready Logic and Fail-Safe Timer. An additional feature of this block is an M1 (fetch) cycle status output flip-flop which permits a hidden refresh capability for dynamic RAMs. This feature is not used in the System 6600 configuration.

The Processor logic block provides:

- CPU high level clocks and clock source for serial I/O timing.
- Address, control and data signals for I/O ports and both on- and off-board memory.
- Instruction decode and execution.
- Service of interrupt requests from both on-board and off-board sources.
- Wait states required by slow memory or I/O devices.

The Z80A CPU is software compatible with the 8080 microprocessor and has 80 additional instructions. It has two sets of six 8-bit general purpose registers that can be addressed individually or in pairs. The additional registers and instructions support block transfer and search capability, sophisticated I/O activities and bit manipulation. It has a sixteen-bit program counter that permits direct addressing of 64K bytes of memory. An external stack can be located anywhere in system memory and is used in conjunction with the 16-bit stack pointer to provide almost unlimited subroutine nesting for use with the interrupt system. The external stack is used as a LIFO stack to store and retrieve contents of the program counter, the flags, the six CPU registers, and the accumulator.

The Z80A instruction set can be broken down into the following major groups:

- Load and Exchange
- Block Transfer and Search
- Arithmetic and Logical
- Rotate and Shift
- Bit Manipulation (Set, Reset and Test)
- Jump, Call and Return
- Input/Output
- Basic CPU Control

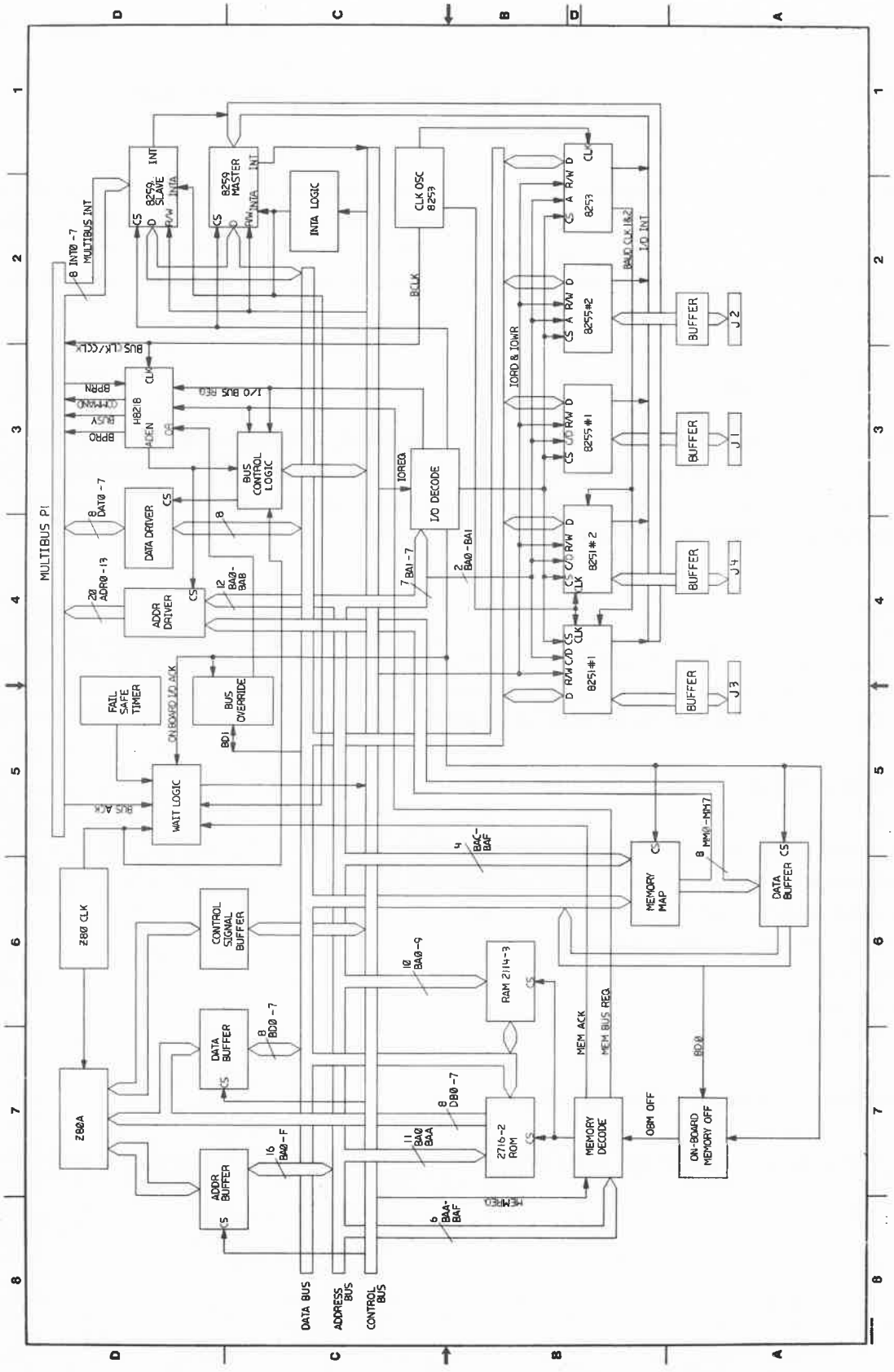


Figure 4-7 System Processor Block Diagram

Memory

The on-board memory consists of 2K ROM/PROM and 2K static RAM (not provided in 6600 System configuration), accessible to the on-board Z80A only. The ROM and RAM occupy the lower 4K address space with the ROM at address zero. The 4K ROM/RAM memory is not mapped and therefore is directly accessible by the Z80A when ROM/RAM OFF is false.

The Z80A also has access to memory on the MULTIBUS and, through mapping, has the capability of accessing a one megabyte memory address space. The memory map consists of 16 entries and provides 4K segment sizes. Since the low 4K on-board memory is not mapped, the Z80A is able to access any 60K bytes of MULTIBUS memory within a one megabyte space at any one time. With ROM/RAM OFF, 64K bytes of MULTIBUS memory are accessable at any one time.

Programmable Interrupt Logic

The interrupt logic serves 8 MULTIBUS interrupts and 7 on-board interrupts when it is enabled by the CPU. Interrupts received are latched, and masked and then the priority is resolved. The Z80 operates in Mode 0 and receives a CALL instruction from the interrupt controllers. The Z80A also has a direct non-maskable interrupt reserved for emergency use.

Input/Output

The Z80A can address up to 256 I/O ports. The addressing of the I/O ports can be direct or indirect. Data transfer can be done in a block fashion capable of handling up to 256 bytes at one time. I/O activities include on-board devices as well as devices on the MULTIBUS.

On-board I/O devices are:

- Two programmable parallel I/O interface controllers (8255)
- Two programmable serial I/O interface controllers (8251)
- Two programmable interrupt controllers (8259)
- Three programmable timers (8253)
- Memory map
- ROM/RAM OFF
- Bus Override

The only MULTIBUS I/O device is Disk Controller.

The specific address assignments and other information for these devices are provided in Chapter 5 of this manual.

Bus Interface

The bus interface has all of the standard MULTIBUS features. These are summarized below:

- Twenty address lines which connect to off-board memory and I/O devices.
- Eight data lines that form a bidirectional bus. This bus transfers data between the CPU, memory and the I/O ports.
- The following control, timing, and interrupt lines:

  Bus Clock - BCLK/
  Bus Priority In - BPRN/
  Bus Busy - BUSY/
  MEMORY READ - MRDC/
  MEMORY WRITE - MWTC/
  I/O READ - IORC/
  I/O WRITE - IOWC/
  XFER ACK -XACK/
  Common Bus Request - CBRQ/
  INITIALIZE - INIT/
  INTERRUPT REQ - INTR0/ to INTR7/

The interface meets the Intel Application note 9800683-02, "Intel Multibus Interfacing".

4.4.5 BLC-064 RAM Memory Board Description

The BLC-064 RAM Memory Board provides 64K bytes of dynamic RAM storage for main memory in the 6600 System. The RAM Memory Board interfaces with the CPU and controller board directly through the system bus. Although the BLC-064 can operate in either an 8-bit or 16-bit mode, the 8-bit mode is used in the 6600 System application.

Separate control circuits on the board initiate the refresh cycle and operate the timing signals used to synchronize read/write functions.

Physical Description

The RAM Memory Board is a double-sided printed circuit board measuring 12 x 6-3/4 inches. The board plugs into the logic Module card cage. It has two edge connectors configured as follows:

- P1 is the on-board MULTIBUS interface connector.
- P2 is reserved for production test points and other National BLC standard signals.

Functional Description

The functional organization of the 64K RAM board is shown in the block diagram, Figure 4-8. The 64K RAM board contains the following major functional blocks:

- Address Control
- Memory Storage
- Operational Control
- Data Input/Output Control

The RAM board provides the system with 64K bytes of read/write memory contained in four banks. Three tri-state bidirectional buffer/latches interface all data in or out of the memory banks to the system bus. All command, address, and data signals to the bus are TTL-level signals. When a command is received from the system bus, the RAM board reads data from, or writes data into, the addressed RAM bank storage location. The read and write operations are accomplished in a similar manner except for the direction of data flow. Bidirectional data buffers are integrated with a latching network which controls the high data byte (for odd addresses) and low data byte (for even addresses). A read or write function accesses a single 8-bit byte by addressing one storage location in each RAM chip within the selected memory bank.

Address decoding occurs prior to reading or writing data. The address is provided by 20 address lines. The RAM location where data is to be read from, or written into is selected by the address control logic which determines the bank location, row, column, and boundary addresses. All timing and control signals for data transfers and refresh originate from on-board logic which is activated by read/write/refresh commands.

The typical read/write cycle time is 495ns. The worst case read/write cycle time is 660ns. Since the RAM elements are required to be refreshed at regular intervals, the refresh cycle time of 615n is generated by on-board logic circuits at 13 usec intervals.

Address Control

The Address Control logic decodes 20 address bits, ADR0/ - ADR13/ which select the board location, RAM bank location, row/column chip locations and boundary address blocks assigned for the board. The address control is described in the following paragraphs.

Seven address bits, ADR1/ - ADR6/ and ADRE/, decode the row address in the selected RAM bank. Seven address bits, ADR7/ - ADRD/, decode the column address in the selected RAM bank. Two address bits, ADRE/ - ADRF/, decode the high-order boundary selection of the 16K address blocks. Four address bits, ADR10/ - ADR13/, decode the highest-order boundary selection of the 64K address blocks within the one megabyte address space.

One address bit, ADR0/, is the least significant address bit which interacts with the Byte High Enable (BHEN/) signal to control the transfer of high/low data bytes for odd/even addresses in the memory array.

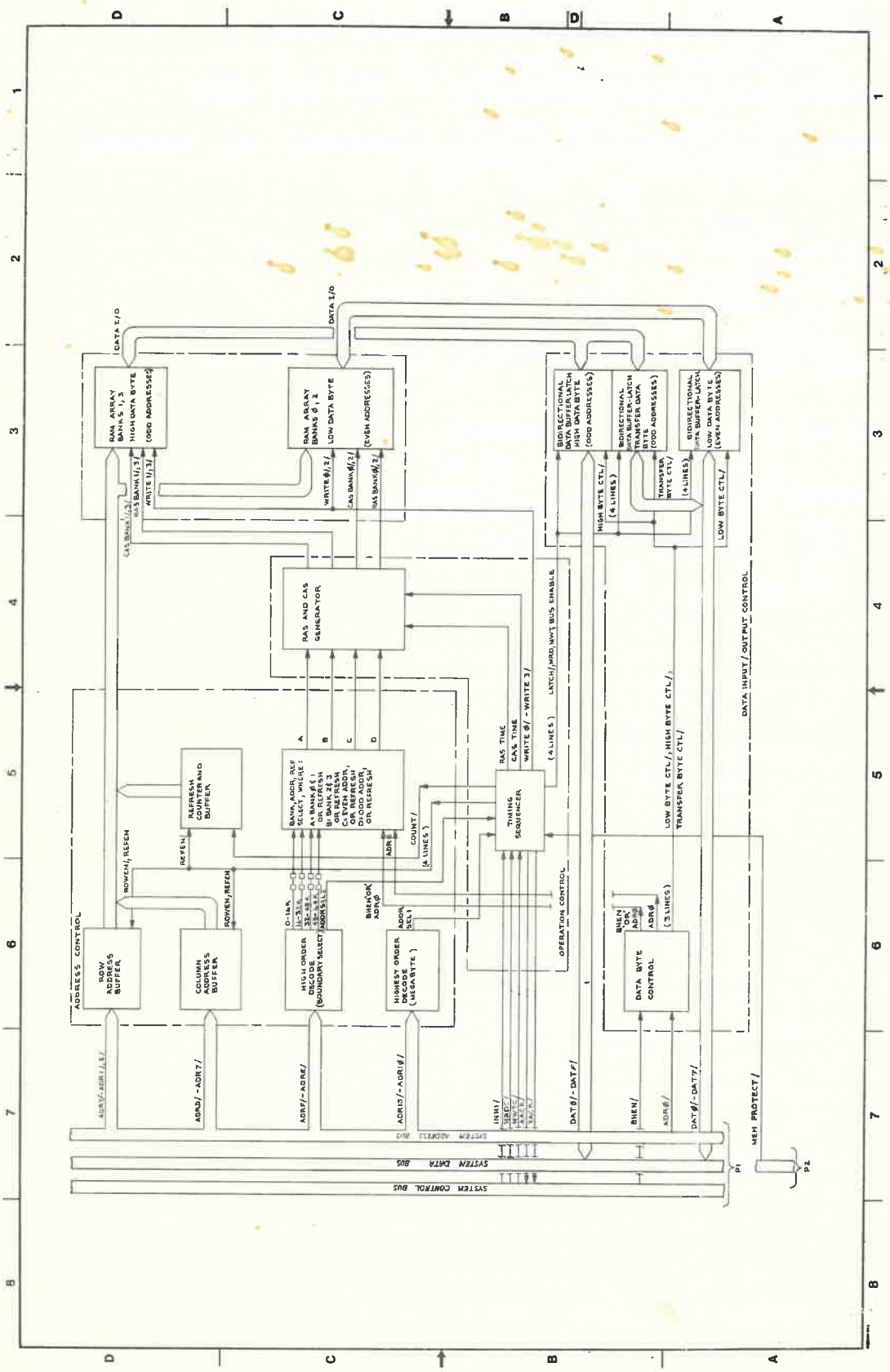

RAM ARRAY BANKS 1, 3 HIGH DATA BYTE (ODD ADDRESSES)
RAM ARRAY BANKS 0, 2 LOW DATA BYTE (EVEN ADDRESSES)
DATA I/O
BIDIRECTIONAL DATA BUFFER/LATCH HIGH DATA BYTE (ODD ADDRESSES)
BIDIRECTIONAL DATA BUFFER/LATCH TRANSFER DATA BYTE (ODD ADDRESSES)
BIDIRECTIONAL DATA BUFFER/LATCH LOW DATA BYTE (EVEN ADDRESSES)
RAS AND CAS GENERATOR
REFRESH COUNTER AND BUFFER
TIMING SEQUENCER
ROW ADDRESS BUFFER
COLUMN ADDRESS BUFFER
HIGH ORDER DECODE (BOUNDARY SELECT)
HIGHEST ORDER DECODE (1MEGABYTE)
DATA BYTE CONTROL
ADDRESS CONTROL
DATA INPUT/OUTPUT CONTROL
SYSTEM ADDRESS BUS
SYSTEM DATA BUS
SYSTEM CONTROL BUS
MEM PROTECT/
P1
P2

Figure 4-8 BIC-064 RAM Block Diagram

Memory Storage

The BLC-064 RAM array contains 32 socketed memory chips which are arranged in four banks with eight chips per bank. The banks are numbered 0 through 3. Thirty-two MM5290 chips provide 16K x 1 bit storage each in RAM banks 0, 1, 2, and 3 to yield a maximum of 64K bytes for the RAM array.

The read or write function accesses a single 8-bit byte by addressing one storage location at each chip within the selected bank. Jumpers are installed on the board to assign 16K address blocks within the array to establish the RAM base address and address boundaries.

Operational Control

The operational control block directs the overall read/write/refresh operation. This logic receives the read/write commands, MRDC/ and MWTC/ from the system control bus and sequences the timing and control signals to access the RAM storage for reading data from, or writing data into the addressed memory bank.

The control function also initiates refresh cycling and generates the RAS/CAS/WRITE timing strobes that are sent to the selected RAM bank. The refresh cycling occurs at 13 usec intervals when a command is not being executed. The refresh logic can also detect the status of the CPU M1 (fetch) state and will initiate a refresh cycle during the 600ns delay period when the CPU is decoding the fetched instruction. This capability is not used in the 6600 System configuration.

The control function also gates the output acknowledge signal, XACK/ to the system control bus when valid read data is presented to the data bus or when valid write data on the bus has been written into the RAM chips.

Data Input/Output

Data input/output control between the system data bus and RAM board is provided by three bidirectional data buffer latches and the high/low multibyte transfer control logic which channels data to or from the selected odd/even RAM bank addresses for high/low data bytes.

The low data byte content, DAT0/ - DAT7/, is gated to or from the even addresses in RAM Banks 0 and 2 by the latch controls of the low byte bidirectional buffer which interface with the system data bus. The high data byte content, DAT8/ - DATF/ is gated to or from the odd addresses in RAM Banks 1 and 3 by latch controls of the high byte bidirectional buffer or transfer byte bidirectional buffer which interfaces with the system data bus.

The multibyte transfer control logic detects the least significant address bit (ADR0/) and the state of the byte high enable signal (BHEN/) to swap 8-bit bytes between the odd and even address locations in the RAM banks. The BHEN/signal is inactive when the 8-bit mode is used.

4.4.6 BLC-8222 Diskette Controller Board Description

The BLC-8222 is an intelligent flexible disk controller board which provides communication between the System Processor and the floppy disk drives. The controller board interacts with the system bus to control all input and output data that is transferred between the disk drive and system bus.

The controller board is capable of selecting one of up to four flexible disk drives. The disk drives accommodate standard (8-inch diameter) diskettes, and, depending upon the system configuration, may contain either single-side or double-side recording surfaces. The single-side and double-side drive types cannot be intermixed. On-board jumper connections, set at the factory, adapt the board for the type of drive and diskette used in the 6600 System.

All data transfer operations to read from, or write onto, the diskette are initiated by the System Processor which communicates with the controller board by issuing standard I/O read/write commands over the system bus. The controller board responds to the I/O command by taking control of the system bus to service the request and to send status to the System Processor through the I/O interface.

The on-board logic devices include the 8080A Microprocessor for the internal processor unit (IPU), two programmable DMA Controller chips, two Programmable Peripheral Interface chips and a Floppy Disk Controller chip. The on-board logic provides the internal control to activate appropriate drive interface lines which interrogate the drive status, control the positioning of read/write heads, perform the necessary serial-to-parallel (and vice versa) conversion of data and transfer the data between the system bus and disk drive.

All of these operations are performed by the controller board logic without intervention from the System Processor. The on-board IPU controls all board operations from the time that the controller board assumes control of the system bus until it completes executing the command and relinquishes the bus to the System Processor. This on-board intelligence relieves the operating system software from the disk operation utility routines which would otherwise increase the system memory requirements and I/O response time.

The BLC-8222 firmware can select either Modified Frequency Modulation (MFM) Format or Frequency Modulation (FM) Format encoding scheme to read from, or write onto the diskette with data ID marks. The encoding scheme can also be changed between FM/MFM mode under program control.

The MFM format corresponds to IBM System 34 Format and is used for double density mode. The MFM format provides a transfer rate of 500K bits/second with 1 million bytes of formatted data by using two disk drives with single-sided diskettes in a system. The FM format corresponds to IBM System 3740 Format and is used for single density mode. Program control of the FM/MFM encoding scheme allows the controller board to perform data transfers for both single and double density diskettes intermixed in the same subsystem.

Additional features of the BLC-8222 include complete cyclic redundancy checking (CRC) and on-board firmware with test routines that permit a user to troubleshoot system problems.

Physical Description

The BLC-8222 is fabricated on a four-layer printed circuit board measuring 12 X 6-3/4 inches. The board plugs into the logic module card cage. The board contains five edge connectors which are configured as follows:

- P1 is the on-board MULTIBUS interface connector
- P2 is reserved for production test points and other National BLC standard signals
- J2 is the connector for four standard (8-inch diameter) floppy disk drives
- J3 is the connector for two miniature (5 1/4-inch diameter) floppy disk drives
- J4 is the connector for two miniature (5 1/4-inch diameter) floppy disk drives

Functional Description

The functional organization of the Diskette Controller board is shown in the block diagram, Figure 4-9. The Diskette Controller board consists of the following major functional blocks:

- External Communication
- Direct Memory Access (DMA)
- Internal Processor Unit (IPU)
- Internal Memory
- Programmable Peripheral Interface (PPI)
- Floppy Disk Controller (FDC)

The basic function of the BLC-8222 logic is to interact with the external system bus and control the transfer of input/output data that passes between the board and the bus. The on-board logic also controls the read/write operations at the external disk drives.

External Communications

The external communications block provides the interface between the controller board and activity on the external system bus. This circuit block includes a Bus Comparator chip, a Bus Controller chip, and two Dual In-line Package (DIP) switches, S1 (Interrupt Select) and S2 (Base Select), that are used to decode addresses and I/O commands. The Bus Controller chip provides control of system bus access, arbitrating bus requests with a similar circuit on the System Processor board. Serial bus priority resolution is used.

Direct Memory Access

The DMA section is comprised of two Programmable DMA Controller chips that are designated as DMA1 and DMA2. DMA1 is used to transfer data blocks between the floppy disk drive and the on-board Internal Memory Section, and between on-board memory and Port A of the Programmable Peripheral Interface (PPI) Section. DMA2 is used for transfers between the external system main memory and Port A of the PPI Section.

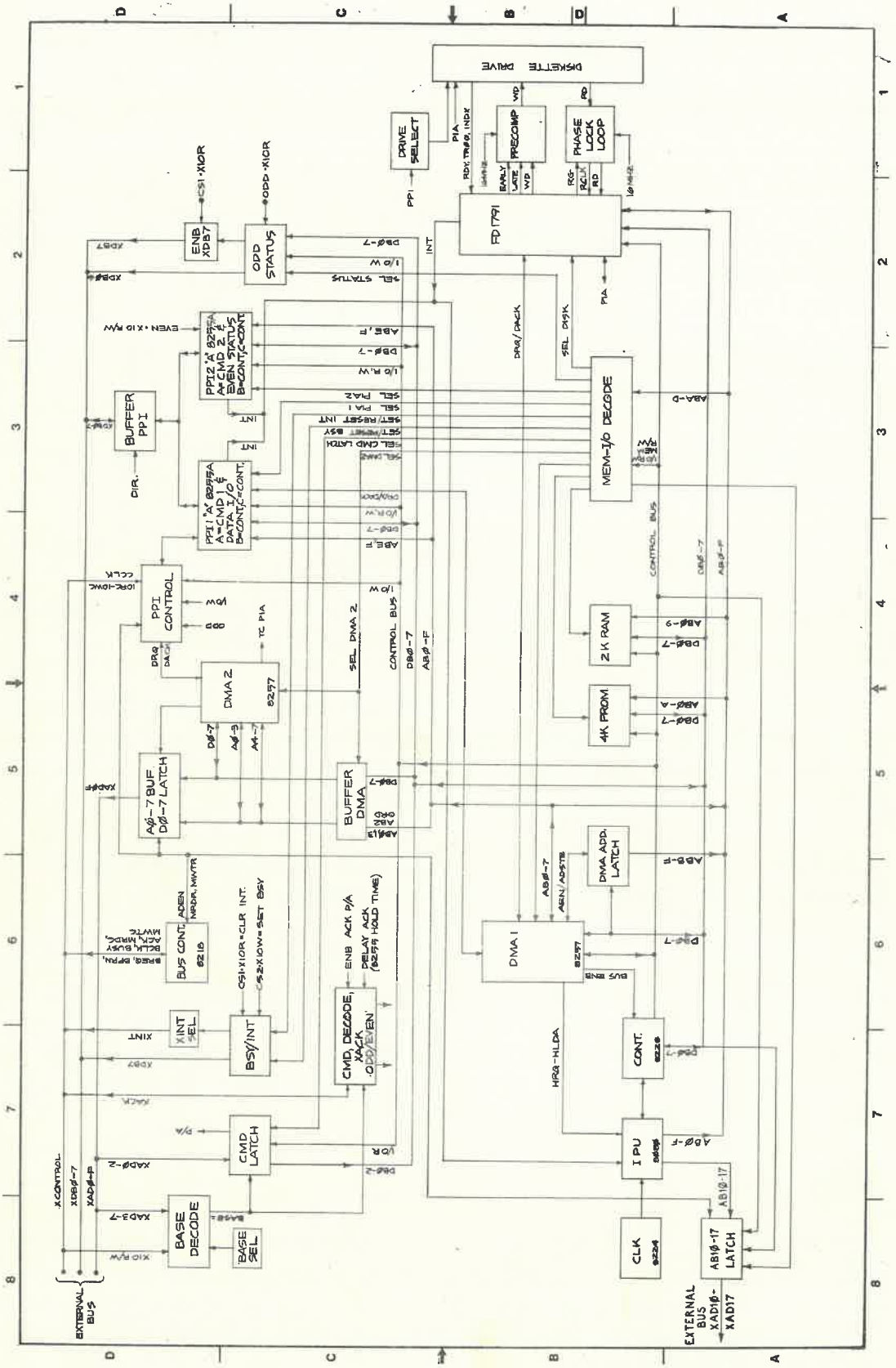


Figure 4-9 BLC-8222 Disk Controller Block Diagram

Internal Processor Unit

The IPU block contains an 8080A microprocessor, a System Controller and Bus Driver chip and a Clock Generator and Driver chip. The IPU section controls all internal I/O ports by accessing the firmware program residing in the on-board PROM.

Internal Memory

The Internal Memory block contains the RAM and PROM memory circuits that are accessed by the IPU for controlling the board operations.

The RAM memory consists of four MM2114 Random Access Memory chips that provide a total of 2K bytes of RAM storage. The RAM is used as a working storage to store variable data for the IPU Section and as a data buffer between the disk and external system memory.

The PROM memory consists of two MM2716 Read Only Memory chips that provide a total of 4K bytes of PROM storage. The PROM is used to store firmware routines.

Programmable Peripheral Interface

The PPI block is software controllable and contains two Programmable Peripheral Interface chips which are designated as PPI-1 and PPI-2. Each chip has three I/O ports (A, B and C).

The A port on each chip is used as a bidirectional register for external communications with the System Processor and System Memory. The A port performs a dual function for command mode and data mode operation to provide status to the System Processor, interrogate commands from the System Processor, and retain data for DMA transfer between the board and System memory.

Port B and C registers on each chip are used to operate in an internal command and status mode to monitor and control the Floppy Disk Controller Chip (FDC) and operate the A ports.

When programmed in the command mode, the IPU can address each PPI to receive the I/O Parameter Block (IOPB) address high and low. In the data mode, the A port register of PPI-1 will hold the data that is transferred between the internal and external memory, while the A port register of PPI-2 will hold the even status for the System Processor. The B port registers of PPI-1 and PPI-2 are used for internal status and commands that originate from the board logic. The C port register of PPI-1 is used for handshaking and controlling the A port registers.

Floppy Disk Controller

The FDC block controls the exchange of data transfers that occur between the BLC-8222 and the external disk drives. The FDC control is provided by an FD1791 Floppy Disk Formatter/Controller chip. This chip accommodates either single or double density formats. It also provides control for single-level write precompensation data, address mark detection and generation, FM/MFM encode and decode logic and track seeking with verification.

The FDC operations are initiated by the firmware to control the movement of the read/write head on a drive, load the head on the diskette and format the data that is transferred to and from the selected disk drive. Separate on-board logic is provided between the disk drive and FDC chip which uses a phase-locked oscillator (PLO) circuit for the synchronization of read data, and a single-level precompensation circuit for write data. Write precompensation occurs for double density only at track location 32 (or greater) for standard size disks, and at track location 16 (or greater) for miniature size disks.

4.5 DISKETTE DRIVE MODULE EQUIPMENT DESCRIPTION

The Diskette Drive module consists of a 19-inch rack mountable electronic assembly which is constructed of the following items:

- Two Sheet Metal Parts (Chassis and Cover)
- Two Shugart Associates (SA800) Diskette Drives (or equivalent)
- Disk Drive DC Power Supply
- AC Fan (70 CFM)
- 50-Conductor Ribbon Signal Cable
- Corcom Line Filter and Fuse Module
- AC/DC Internal Power Harness
- Lighted Power Switch

AC input power is provided to the module through an external power cord which is plugged into a power receptacle at the rear of the module. A lighted ON/OFF power switch is provided on the module front panel. A fuse receptacle and a factory set voltage selector are provided on the rear of the module at the power receptacle connection. A 50-pin ribbon panel connector is provided on the rear of the module for connection to the disk controller located within the Logic Module assembly. Two labels, 'A' and 'B', are provided on the module front surface to designate the two disk drives as referenced by the system software.

The AC/DC power and signal routing within the module are shown in Figure 4-10.

As shown, the AC input power - after the fuse, line filter, and ON/OFF switch - is distributed to the Disk DC Power Supply, the Disk Drives ('A' and 'B'), and the fan. The DC Power Supply provides the DC power required by the two disk drives. The 50-conductor ribbon cable within the module provides a point-to-point signal interface between the two disk drives and the panel mount connector located on the rear of the module. The difference between drive 'A' and 'B' is the configuration of the Berg jumpers on the drives which determine the drive select response and the signal bus terminating resistors. Drive 'A' is jumpered for 'Drive Select 1', and Drive 'B' is jumpered for 'Drive Select 2'. Drive 'B' is also jumpered to provide signal terminators T3 through T6 on the Shugart drive.

The signal interface to the disk drive is the industry standard as used by Shugart Associates and other manufacturers. The specific internal pin assignment is as indicated in Table 4-11. The mating connector for the panel mount connection is 3M P/N 3564-1001.

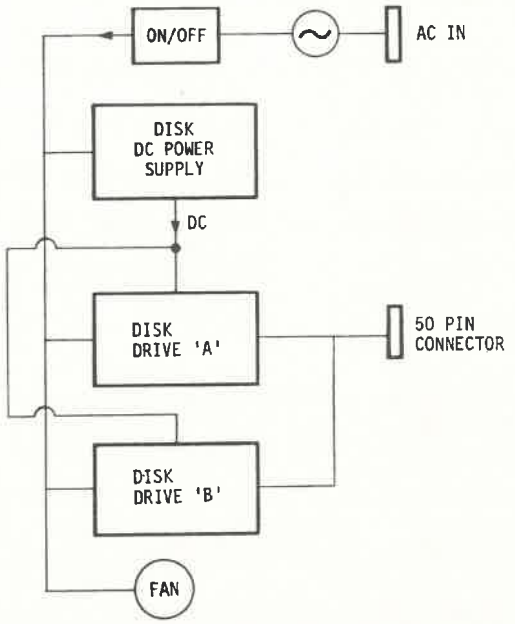


Figure 4-10 Diskette Drive Module AC/DC Power and Signal Routing

TABLE 4-8 DISK DRIVE SIGNAL INTERFACE PIN ASSIGNMENTS

SIGNAL NAME	SA800		PANEL CONNECTOR	
	PIN	RETURN	PIN	RETURN
DISK CHANGE	12	11	6	31
IN USE *	16	15	8	33
HEAD LOAD *	18	17	9	34
INDEX	20	19	10	35
READY	22	21	11	36
SECTOR *	24	23	12	37
DRIVE SELECT 1	26	25	13	38
DRIVE SELECT 2	28	27	14	39
DRIVE SELECT 3 *	30	29	15	40
DRIVE SELECT 4 *	32	31	16	41
DIRECTION SELECT	34	33	17	42
STEP	36	35	18	43
WRITE DATA	38	37	19	44
WRITE GATE	40	39	20	45
TRACK 00	42	41	21	46
WRITE PROTECT	44	43	22	47
READ DATA	46	45	23	48
SEP DATA *	48	47	24	49
SEP CLOCK *	50	49	25	50

*Signal not used by BLC-8222 Disk Controller.

4.5.1 Drive Power Supply

The DC power supply provides the following DC output for the two drives:

+5VDC,	2.5A	
-5VDC,	0.5A	
+24VDC,	3.0A	Avg/3.4A Peak

4.5.2 Drive Description

General Operation. The SA800 Diskette Drive consists of read/write and control electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette. These components perform the following functions:

- Interpret and generate control signals.
- Move read/write head to the selected track.
- Read and write data.

The relationship and interface signals for the internal functions of the SA800 are shown in Figure 4-11.

The Head Positioning Actuator positions the read/write head to the desired track on the diskette. The Head Load Actuator loads the diskette against the read/write head; data may then be recorded or read from the diskette.

Read/Write and Control Electronics. The electronics are packaged on one PCB. The PCB contains:

- Index Detector Circuits
- Head Position Actuator Driver
- Head Load Actuator Driver
- Read/Write Amplifier and Transition Detector
- Write Protect
- Drive Ready Detector Circuit
- Drive Select Circuits

Drive Mechanism. The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accomplished at the factory with different size drive pulleys and belts. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

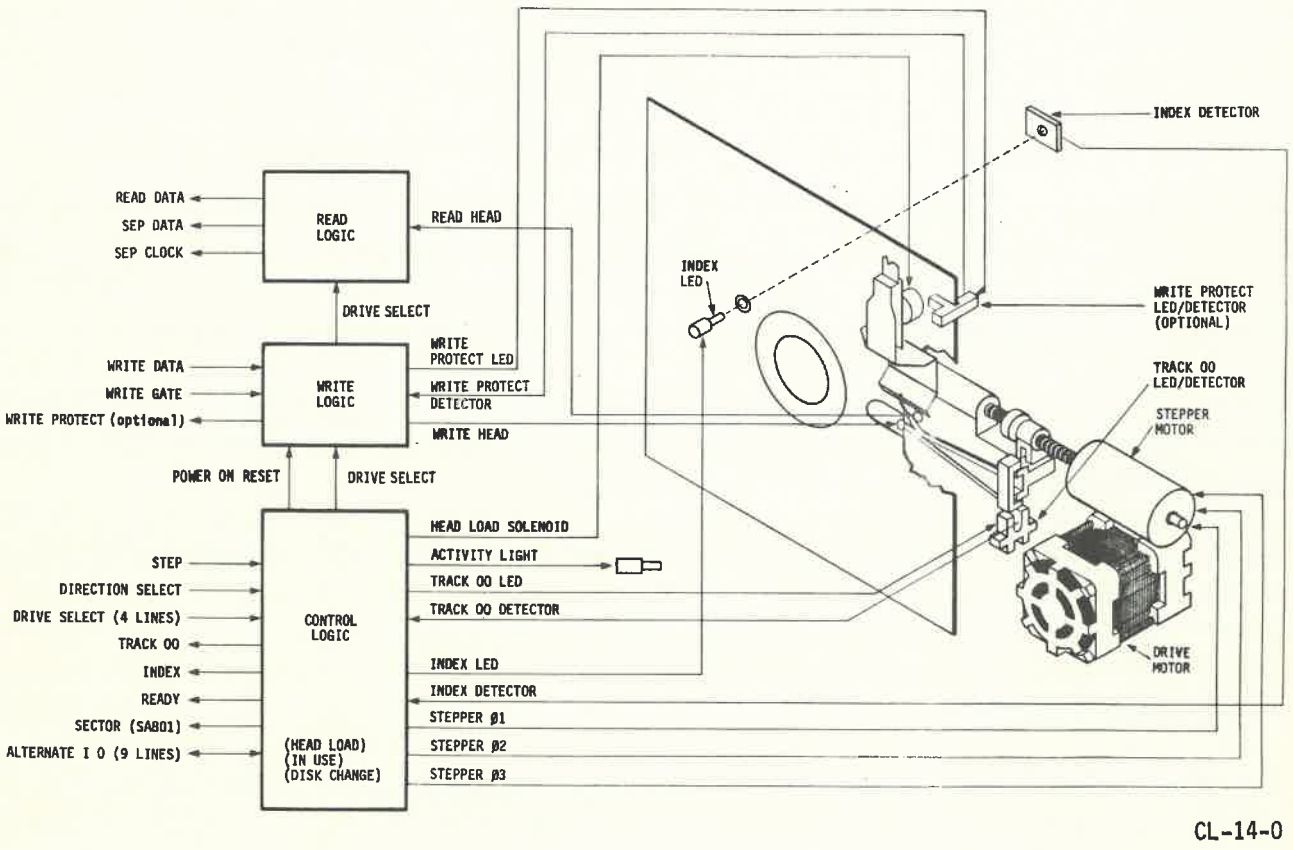


Figure 4-11 SA800 Functional Diagram

Positioning Mechanism. An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw head. The stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

Read/Write Head. The SA800 head is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal-to-noise ratio. This insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Actuator lead screw. The Diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.

The read/write head is in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

Recording Format. The format of the data recorded on the disk for use in the MICROSYSTEM 6600 is described in subsection 4.6.2.

4.5.3 Signal Interface

The signal interface to the module contains both control and Data Transfer lines. All lines in th signal interface are digital in nature and either provide signals to the drive (input), or provid signals to the disk controller output, via interface connectors P1/J1 on the disk drives.

Input Lines

There are ten signal input lines, eight are standard and two are configured options.

The input signals are of two types, those which are multiplexed and those which perform the multiplexing. The multiplexed input signals are:

- Direction Select
- Step
- Write Data
- Write Gate

The input signals which perform the multiplexing are:

- Drive Select 1
- Drive Select 2
- Drive Select 3 (unused)
- Drive Select 4 (unused)

The input lines have the following electrical specifications.

- True = Logical zero = Vin $\pm$ 0.0V to 0.4V @Iin = 40 ma (max)
- False = Logical one = Vin +2.5V to +5.25V @Iin = 0 ma (open)
- Input Impedence = 150 ohms

Input Line Termination

The SA800 is provided with the capability of terminating the four input lines, which are multiplexed, by jumpering traces. These four lines and their respective jumpering traces are:

- Direction Select ..... Trace T3
- Step ..... Trace T4
- Write Data ..... Trace T5
- Write Gate ..... Trace T6

In order for the drive to function properly, the last drive on the interface must have these four lines terminated. Termination of these four lines can be accomplished by one of the two following methods:

1. As the system is shipped from the factory, jumpers are installed on the terminator ports T3, T4, T5, and T6 on drive B within the module. Remove these shorting plugs from any additional drives which are added to the configuration.

2. External termination may be used provided the terminator is beyond the last drive. Each of the four lines should be terminated by using a 150 ohm, 1/4 watt resistor, pulled up to +5 V_{CC} and jumpers T3 through T6 should be removed from drive B.

Drive Select 1-4. Drive Select when activated to a logical zero level, activates the multiplexed input lines and loads the R/W head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines are provided so that up to four drives may be multiplexed together in a system and have separate Drive select lines. Traces DS1, DS2, DS3, and DS4 have been provided to select which Drive select line activates the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on either DS1 or DS2 depending upon the drive location within the module.

Direction Select. This interface line is a control signal which defines direction of motion the R/W head takes when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head moves away from the center of the disk Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the R/W head moves towards the center of the disk.

Step. This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line. The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse.

Write Gate. The active state of this signal, logical zero, enables write Data to be written on the diskette. The inactive state, logical one, enables the read data logic (Seperated Data, Separated Clock, and Read Data) and stepper logic.

Write Data. This interface line provides the data to be writtin on the diskette. Each transition from a logical one level to a logical zero level causes the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active.

In Use. This customer installed option, when enabled by jumpering Trace D and activated to a logical zero level turns on the Drive Busy LED in the push button. This is an "OR" function With Drive Select. (Signal not used in 6600 System)

Output Lines

There are six standard and two optional output lines from the SA800. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 mA at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is off, the collector current is a maximum of 25 microamperes.

Trace 00. The active state of this signal (logical zero) indicates when the drive's R/W head is positioned at track zero (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. The signal is at a logical one level, or false state, when the selected drive's R/W head is not at track 00.

Index. This interface signal is provided by the drive once each revolution (166.67 ms) of the diskette to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.7 ms once each revolution.

Ready. This interface signal indicates that two index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of +5V power to the drive.

Read Data. This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is at a logical one level and becomes a logical zero level for the active state.

Sep Data. This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is at a logical one level and becomes a logical zero level for the active state. (Signal not used in 6600 System)

Sep Clock. This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. (Signal not used in 6600 System)

Write Protect. This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is at a logical zero level when write protected. Under normal operation, the drive inhibits writing with a protected diskette installed, in addition to notifying the interface.

Disk Change. This option is installed in the factory shipped configuration. It provides a true signal (logical zero) to the interface (pin 12) when Drive Select is activated if, while deselected, the drive has gone from a Ready to a Not Ready (Door Open) condition. This line is reset on the true to false transition of Drive Select if the drive has gone Ready.

4.6 LOADER OPERATION

The MICROSYSTEM 6600 is loaded via two loader programs; a firmware program, called the Boot Firmware, resident in PROM on the System Processor board and a loader program, called the System Loader, resident on track 0 of both the system diskette and diagnostic diskette. The boot firmware serves to initiate operation of the system CPU and load the system loader from disk. The system loader then completes the loading operation.

4.6.1 Hardware Requirements

The operation of the boot firmware requires the following MICROSYSTEM 6600 hardware configuration:

- BLC-8222 Flexible Disk Controller Board
- Z80A Based System Processor Board

- BLC-064 RAM Board
- System Terminal Device (CRT Terminal)

4.6.2 Diskette Requirements

To operate with the boot firmware (so that loading and transfer of control to the diskette based system loader can occur) the diskette format must comply with either the MICROSYSTEM 6600 CP/M System diskette format or the MICROSYSTEM 6600 Diagnostic diskette format. The specific format requirements are as follows:

a. Track 0 must be single-density. The sector length may be either 128 bytes or 256 bytes.

b. Sector 1 on track 0 must contain a boot loader program that meets the following requirements:

   i) The twentieth byte must contain 21H and the twenty-third byte must contain B6H.

   ii) Control is transferred to the twentieth byte within the system loader program, which is loaded at location 1000H. Therefore, the logical flow of the program must start at this displacement.

c. Subsequent tracks may be single- or double-density depending on the specific application. The MICROSYSTEM 6600 CP/M diskette is double-density with 512 byte sectors. The MICROSYSTEM 6600 diagnostic diskette is also double-density but the sectors are 256 bytes.

4.6.3 Boot Firmware Program Description

The boot firmware program is assembled in a single 2716-2 PROM occupying memory locations 0000H through 07FFH on the System Processor board. The program is invoked when the board receives a reset signal. The active reset signal enables access to the PROM and sets the CPU program counter to 0000H. This starts execution of the boot firmware program. The reset signal can be generated either at power-up or when the front panel RESET switch is pressed.

The boot firmware program provides two entry points so that user's programs can return control, if required. These are:

- Location 007F2H, for non-error type returns
- Location 007F5H, for loading error returns

The boot firmware program performs the following functions:

- Runs CPU and memory diagnostics to ensure the system is capable of loading from disk.
- Examines the flexible disk controller diagnostic results to ensure proper operation.
- Initializes the CRT serial port to the correct baud rate setting. The program supports the following standard baud rates:

  110 Baud
  300 Baud
  600 Baud
  1200 Baud
  2400 Baud
  4800 Baud
  9600 Baud

- Displays (if possible) any error messages resulting from the first three operations (Boot firmware error messages were given in Table 3-1).
- Reads and verifies the contents of Sector 1, Track 0, of the diskette. Data is read into location 1000H to 10FFH.
- Jumps to location 1020H to pass control to the system loader program just loaded from disk.

Figure 4-12 shows a flow chart of the boot firmware. For more detail on the firmware program refer to Chapter 8.

NOTE: If no diskette is present in the drive during loading, the boot firmware displays the following message:

MOUNT SYSTEM DISK AND HIT RETURN KEY

If a disk is present but not recognized as a properly formatted disk for the MICROSYSTEM 6600, i.e., the twentieth location of track 0, sector 1 is not 21H and the twenty-third location of track 0, sector 1 is not B6H, the boot firmware displays the following message:

NON-SYSTEM DISK

If a disk error occurs while the boot firmware program is reading track 0, sector 1, the following message is displayed:

DISK ERROR

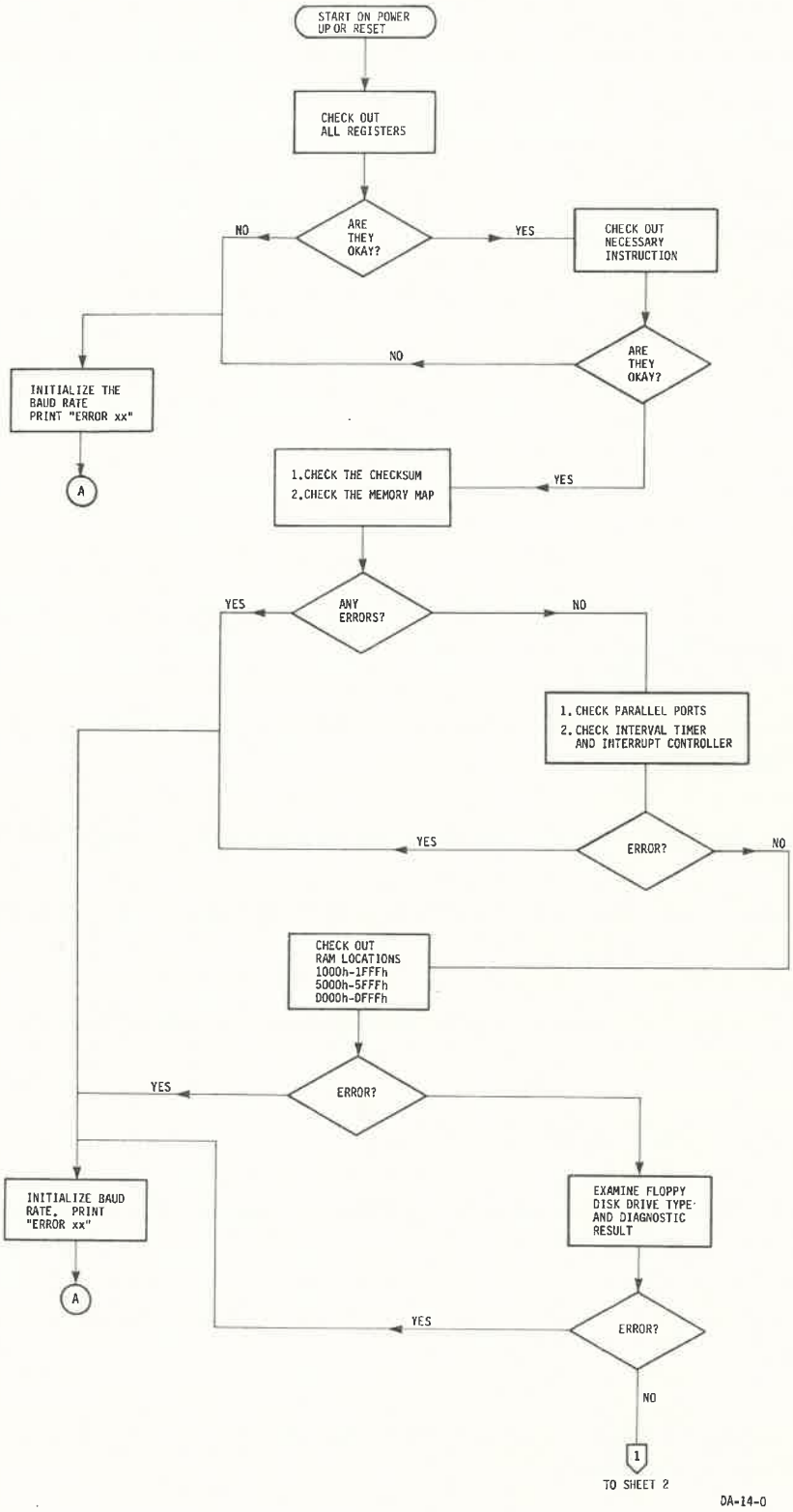


Figure 4-12 Boot Firmware Flow Chart (sheet 1)

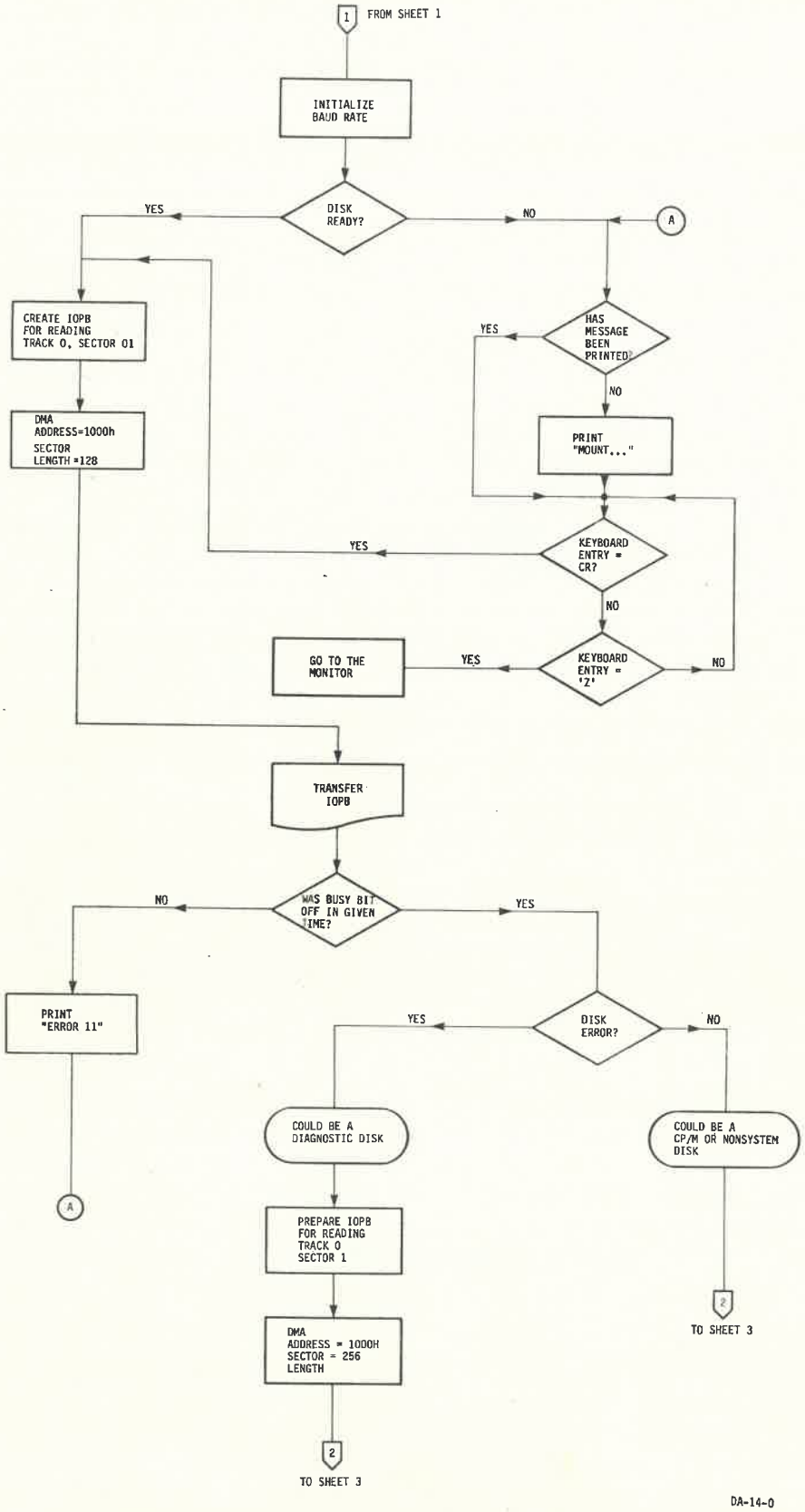


Figure 4-12 Boot Firmware Flow Chart (sheet 2)

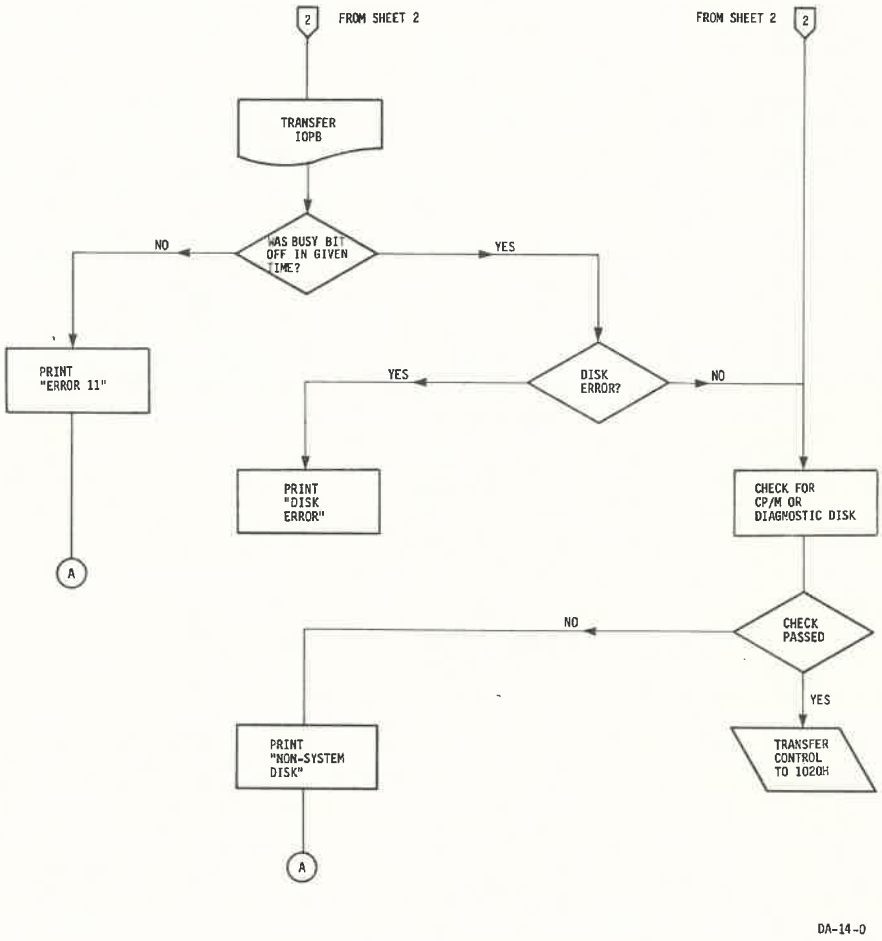


Figure 4-12 Boot Firmware Flow Chart (sheet 3)

4.6.4 System Loader Program Description

The system loader program resides on track 0, sector 1, of the MICROSYSTEM 6600 CP/M system diskette. Once control is passed to the system loader from the boot firmware, the following functions are performed:

- The rest of track 0 is loaded. This consists of 26 sectors, sector length 128 bytes, single density. The sectors are loaded into memory location DF80H onward. If a load error occurs, an error message is displayed (refer to Chapter 3) and control is returned to the boot firmware.

- All of track 1 is loaded. This consists of 9 sectors, sector length 512 bytes, double density. The sectors are loaded into memory location EC80H onward. An unsuccessful load will return control to the boot firmware.

- The disk is checked to see if it is a system disk. This is done by examining six bytes in memory that are within the system BIOS area.

- On success, the PROM is turned off, this operation is verified, and the loader jumps to location F600H.

Figure 4-13 shows a flow chart of the system loader program. Appendix C gives program listings for the system loader.

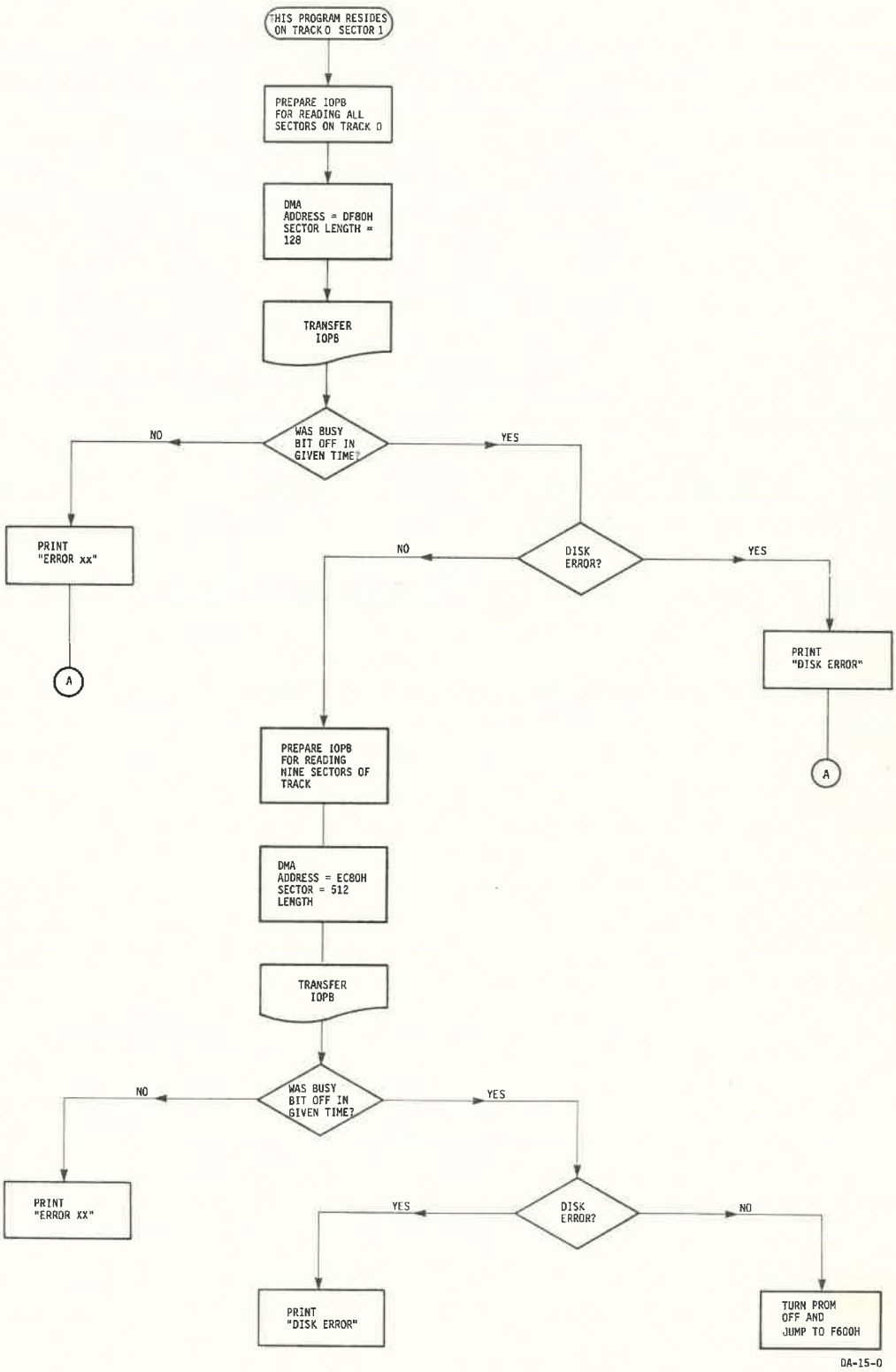


Figure 4-13 System Loader Flow Chart

Chapter 5

SYSTEM PROCESSOR BOARD

5.1 INTRODUCTION

This chapter provides a detailed description of the logic within the System Processor board, and a summary of the Z80A instruction set.

The board contains the following functional areas as shown in Figure 5-1.

- CPU Block
- Memory Block
- Interrupt Block
- Input/Output Block
- Bus Interface Block

5.2 The CPU BLOCK

This block contains the basic logic units shown in Figure 5-1. All central processing and control functions are performed by the CPU block. These functions are:

- Fetch, decode and execute instructions.
- Service interrupts from external or on-board devices.

5.2.1 Z80A CPU

The Z80A CPU is the heart of the entire system. It oversees the control of the other system components. In the following paragraphs the internal structure of the CPU, as shown in Figure 5-2, is discussed. The pin assignments for the Z80A can be found in Appendix I.

The Z80A CPU contains 208 bits of R/W memory that are accessible to the programmer. Figure 5-3 illustrates how this memory is configured into eighteen 8-bit registers and four 16-bit registers. All Z80A registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulator and flag registers.

Special Purpose Registers

1. Program Counter (PC). The program counter holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transfered to the address lines. When a program jump occurs, the new value is automatically placed in the PC, overriding the incrementer.

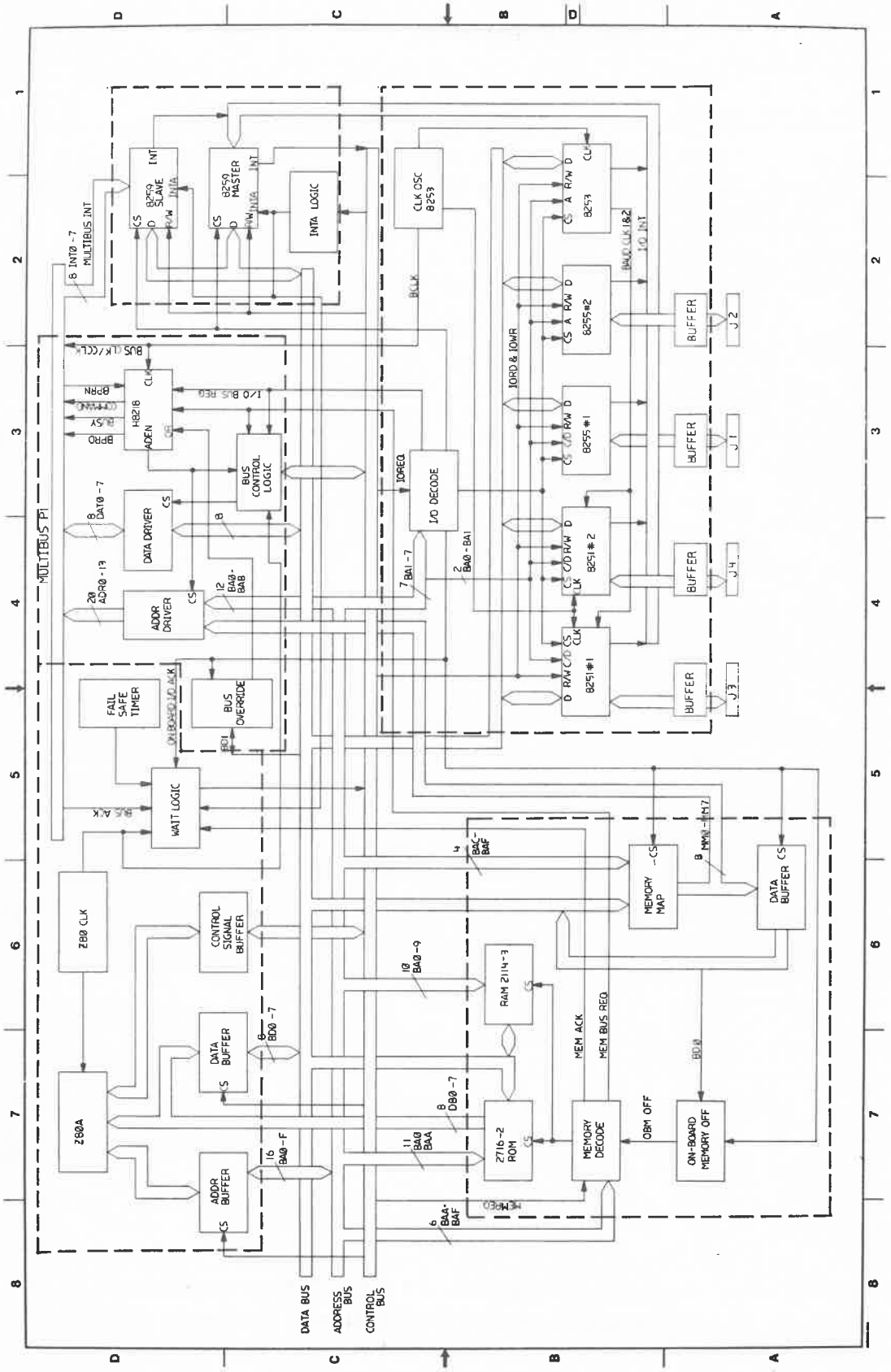


Figure 5-1 System Processor Block Diagram

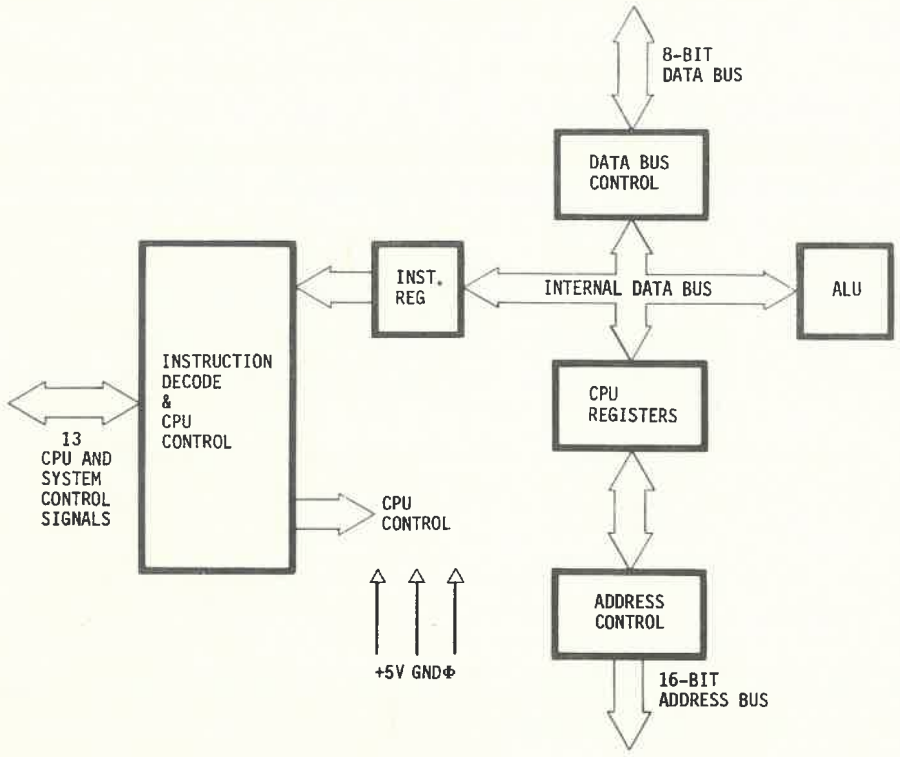


Figure 5-2 Z80 CPU Block Diagram

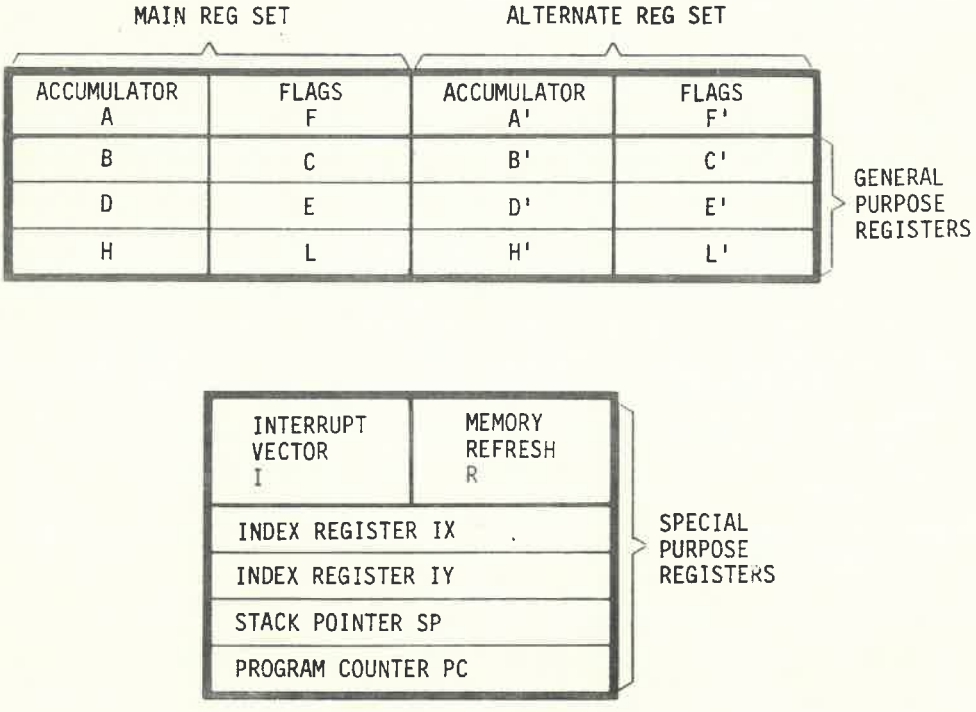


Figure 5-3 Z80 CPU Register Configuration

2. Stack Pointer (SP). The stack pointer holds the 16-bit address of the current top of stack located anywhere in external system RAM memory. The external stack memory is organized as a last-in-first-out (LIFO) file. Data can be "PUSHed" onto the stack from specific CPU registers or "POPped" off of the stack into specific CPU registers through the execution of PUSH and POP instructions. The data popped from the stack is always the last pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data manipulation.

3. Two Index Registers (IX & IY). The two independent index registers hold a 16 bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory where data is to be stored to or retrieved from. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer. This mode of addressing greatly simplifies many types of programs, especially where tables of data are used.

Accumulator and Flag Registers

The CPU includes two independent 8-bit accumulators, each with an associated 8-bit flag register. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16 bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair with a single exchange instruction.

General Purpose Registers

There are two matched sets of general purpose registers each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is call BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers, an accumulator and a flag register may be reserved for handling this very fast routine. Only a simple exchange command need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

Arithmetic and Logic Unit (ALU)

The 8-bit arithmetic and logic instructions of the CPU are executed in the ALU. Internally, the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

Add	Left or right shifts or rotates (arithmetic and logical)
Subtract	Increment
Logical AND	Decrement
Logical OR	Set a bit
Logical Exclusive OR	Reset a bit
Compare	Test a bit

Instruction Register and CPU Control

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control section performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

5.2.2 Failsafe Timer

A jumper controlled failsafe timer is implemented to prevent the CPU from getting into a permanent wait state. This timer is an on-board 10 msec time-out timer. Attempted access to non-existent memory or I/O device, when the Failsafe Timer is disabled results in a permanent system bus hang up. The only recovery from this is a system RESET.

5.2.3 System Clock

The CPU operates on a 3.686 MHz clock. The System Processor board provides Bus Clock and Constant Clock to the MULTIBUS. Three interval timers are provided for timing and control purposes. The clock input to the interval timers has a frequency variation of less than $\pm$ 0.07%.

5.3 MEMORY BLOCK

This block contains the Memory Map, On-board PROM/RAM, and ROM/RAM OFF control logic.

5.3.1 Memory Map

The Memory Map occupies I/O address D7 Hex. Writes to this location are used to set the contents of the sixteen map locations and reads from this location are used to interrogate the map contents. The data path to the map is eight bits wide with the bit assignment as indicated below:

INPUT/OUTPUT

7	6	5	4	3	2	1	0

MULTIBUS ADDRESS LINE 0C Hex
.
.
.
MULTIBUS ADDRESS LINE 13 Hex

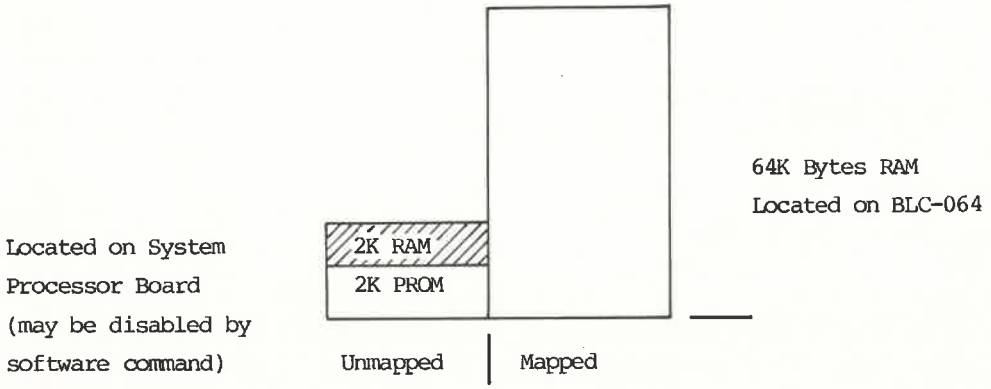
The high four address lines (C, D, E, F) of the system Z80 processor are wired to the map logic. During memory accesses, above the low 4K (ROM, RAM), these lines are used to directly address the contents of the map, and the eight map data output lines are enabled through drivers to drive the high eight MULTIBUS address lines. The map is also used to address the MULTIBUS when the ROM OFF feature disables the on-board ROM/RAM located at the lowest 4K of the address space.

To write and read the contents of the sixteen map locations, the indirect I/O instruciton OUT/IN (C),B is used, where register C contains D7 (the map address) and the upper four bits of register B contain the map segment address.

5.3.2 On-board PROM/RAM

The system memory consists of memory blocks located on the System Processor board, and the BLC-064 RAM board.

The relationship of the memory elements is as illustrated below:

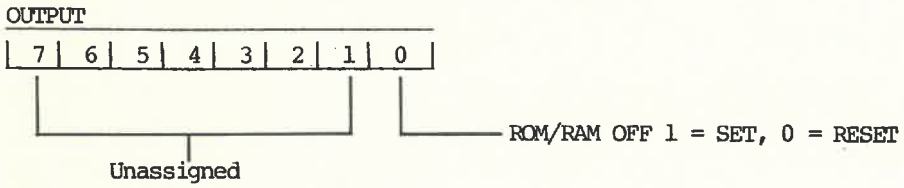


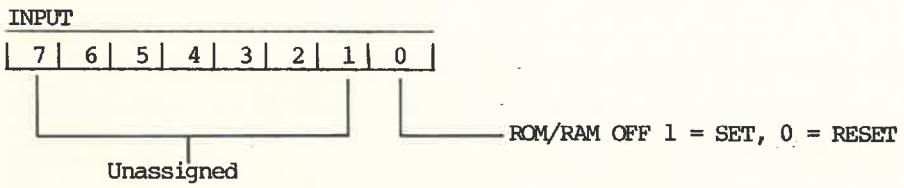
The PROM and RAM (not provided in 6600 System configuration) on the System Processor board are located on the on-board micro bus and are only accessible by the on-board processor. The PROM and RAM are at address zero and occupy the first 4K memory space. The remaining system memory is located on the MULTIBUS and is accessible by the processor through the mapping logic located on the Board. The map segment size is 4K and therefore, the processor has 15 segment elements to use in accessing the mapped memory. A sixteenth segment element is used when on-board ROM/RAM is disabled.

The 64K bytes located on the BLC-064 board are address jumpered to bank zero on the MULTIBUS. The System Processor is able to access the lower 4K within this memory bank by either using the ROM/RAM off capability or by mapping this segment to a higher RAM area within the low 64K RAM space.

5.3.3 ROM/RAM OFF Control Logic

This control logic is set and reset through I/O writes. The ROM/RAM OFF occupies addresses D0-D3. The bit assignment is as indicated below:





Upon power-up or backplane initialization, ROM/RAM OFF is reset. This enables the on-board 4K memory. ROM/RAM OFF set disables the on-board memory; memory space 0 to 4K will be assigned to off-board memory, subject to the memory map.

5.4 INTERRUPT BLOCK

Seven interrupt levels are used by devices located on the System Processor board and the remaining eight levels are provided for MULTIBUS devices. All the interrupts are handled by two 8259 interrupt controllers (edge sensitive) used in cascade mode. The second 8259 is wired as a slave on master interrupt level 3. The on-board devices are connected to the master controller and the MULTIBUS interrupt lines are connected to the slave controller.

5.4.1 Interrupt Assignments

The device interrupt assignments within the system are as shown below:

System Processor Board

0 RS232 #1 RRDY (Receiver Ready)
1 RS232 #2 RRDY (Receiver Ready)

2 Interval Timer (8253)
3 Backplane Interrupt Controller (Slave 8259)
4 RS232 #1 TRDY (Transmitter Ready)
5 RS232 #2 TRDY (Transmitter Ready)
6 Printer Not Busy (8255)
7 Unassigned Parallel Port (8255)

Backplane

0-4 Unassigned
5 Floppy Disk Controller - Not Busy
6-7 Unassigned

For details of interrupt timing refer to the CPU timing section of a Z80A manual.

5.4.2 Interrupt Controllers

The two 8259 Interrupt Controllers are located on the micro bus within the System Processor board and are not accessible from the MULTIBUS. The devices occupy addresses D8 through DB Hex within the CPU I/O space.

Programming of the 8259's by the CPU is accomplished by the generation of two types of command words:

1. Initialization Command Words (ICWs) which enable normal operation by bringing the 8259 to a starting point.

2. Operation Command Words (OCWs) which determine the interrupt mode in which the 8259 will operate. The modes are: Fully nested, Rotating Priority, Special Masked, and Polled. These words can be written into the 8259 at any time.

Initialization Command Words (ICWs)

Initialization consists of the following:

- Resetting the edge sense circuit so that interrupt request inputs must have a low-to-high transition to generate an interrupt.

- Assigning lowest interrupt priority to the IR7 input.

- Resetting the special mask mode flip-flop and status read flip-flop.

As shown in Figure 5-4, ICW1 determines: 1) the three most significant bits (A7, A6, A5) of the service subroutine lower address, 2) whether addresses associated with interrupt request inputs are at equally spaced intervals of eight bytes (containing the entire routine) or four bytes (used to store a Jump instruction when eight bytes are not sufficient to store the routine), and 3) whether there is one or multiple 8259s. The System Processor uses two 8259s, so S is always 0. Table 5-1 shows the lower routine address format for both 4-byte and 8-byte intervals.

ICW1 and ICW2 together supply 10 bits of the address (A15-A6) and the 8259 supplies five bits (A4-A0). ICW1 supplies A5 for 4-byte intervals and the 8259 supplies A5 for 8-byte intervals.

Any command in which A0=0, D0=0 and D4=1 is interpreted by the 8259 as ICW1. The System Processor requires ICW1, ICW2, and ICW3 to control the master-slave relationship of the two 8259s.

A flow diagram for initialization is shown in Figure 5-5. ICW2 must follow as the next command after ICW1. The 8259 can handle interrupt requests in the fully nested mode after ICW2. Note that interrupts must be disabled by a DI instruction from the CPU when this sequence occurs. Interrupts are automatically disabled after the CPU is reset.

In the fully nested mode, IR inputs are automatically assigned priority levels, with IR0 having the highest priority and IR7 the lowest. The 8259 places the address vector of the highest priority interrupt request on the data bus and the ISR bit for that IR input is set, thereby inhibiting further requests of lower priority interrupts from generating interrupts to the CPU. Higher priority interrupts can be generated, but are only acknowledged by the CPU if the CPU has executed an Enable Interrupt (EI) instruction. The ISR bit remains set until an End-of-Interrupt (EOI) is received at the end of the service routine.

Operation Command Words (OCWs)

The 8259 can handle interrupts in the fully nested mode once it has been initialized, but it can be commanded to operate in a variety of other priority modes through the use of Operation Command Words (OCWs).

OCWs provide a choice of algorithms that determine the various priority modes of operation - masked interrupt requests, fully nested, rotate, polling, and special mask modes - as well as the ability to read the status of internal 8259 registers.

The various interrupt modes and the operation command words used to provide them are described below:

OCW1 - Interrupt Mask Control - This command controls the Interrupt Mask Register (IMR). Individual bits at the output of the IMR are set high, thereby preventing Interrupt Request Register (IRR) bits from being processed by the priority resolver. An interrupt can be generated if the IMR bit is reset low while an IRR bit is set.

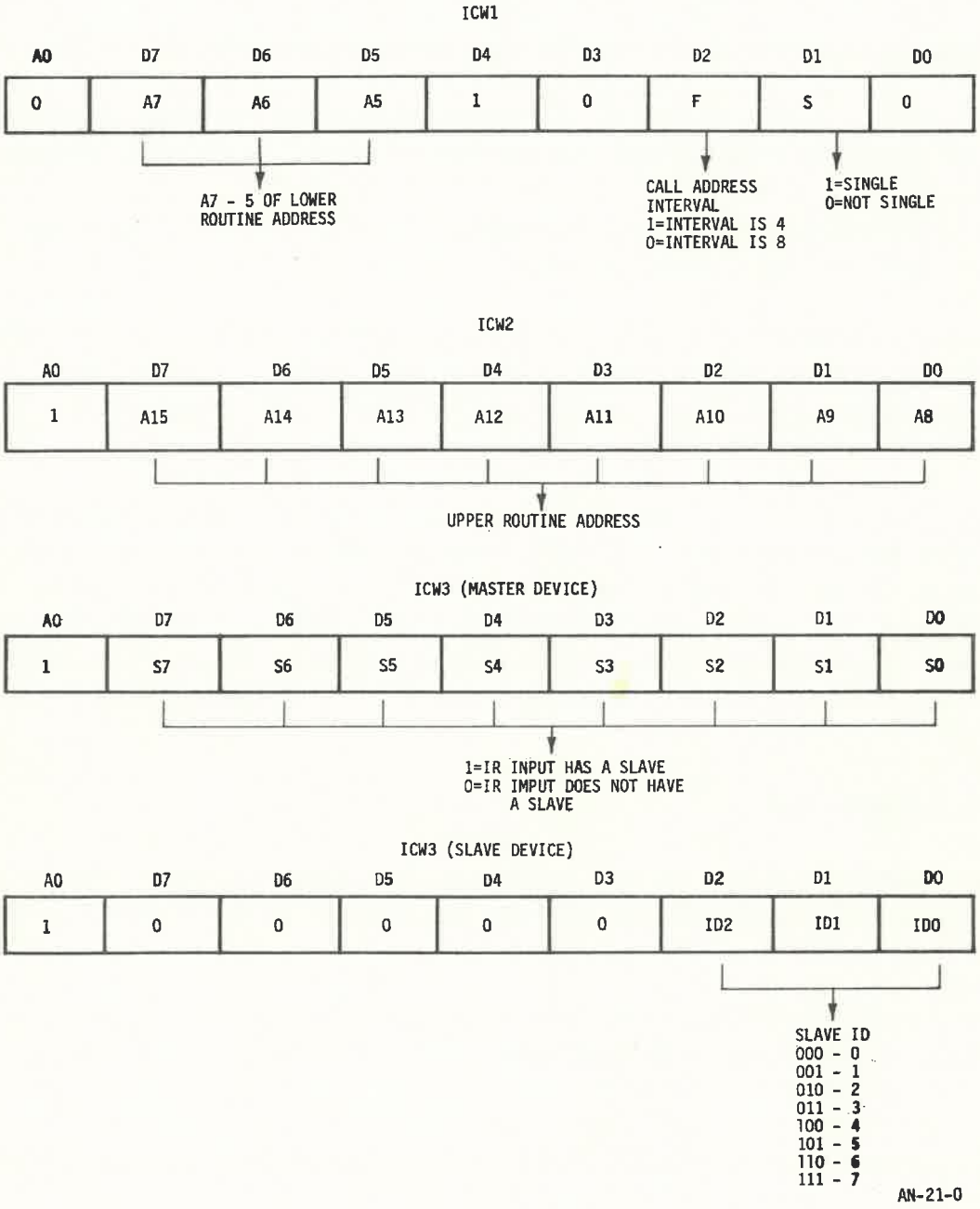

ICW1
A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 0 F S 0
A7 - 5 OF LOWER ROUTINE ADDRESS
CALL ADDRESS INTERVAL 1=INTERVAL IS 4 0=INTERVAL IS 8
1=SINGLE 0=NOT SINGLE
ICW2
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 A15 A14 A13 A12 A11 A10 A9 A8
UPPER ROUTINE ADDRESS
ICW3 (MASTER DEVICE)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 S7 S6 S5 S4 S3 S2 S1 S0
1=IR INPUT HAS A SLAVE
0=IR IMPUT DOES NOT HAVE A SLAVE
ICW3 (SLAVE DEVICE)
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 0 0 ID2 ID1 ID0
SLAVE ID
000 - 0
001 - 1
010 - 2
011 - 3
100 - 4
101 - 5
110 - 6
111 - 7
AN-21-0

Figure 5-4 Initialization Command Word Format

TABLE 5-1 8259 LOWER ROUTINE ADDRESS

INTERRUPT INPUT	INTERVAL = 4								INTERVAL = 8							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR 7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR 6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR 5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR 4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR 3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR 2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR 1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR 0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

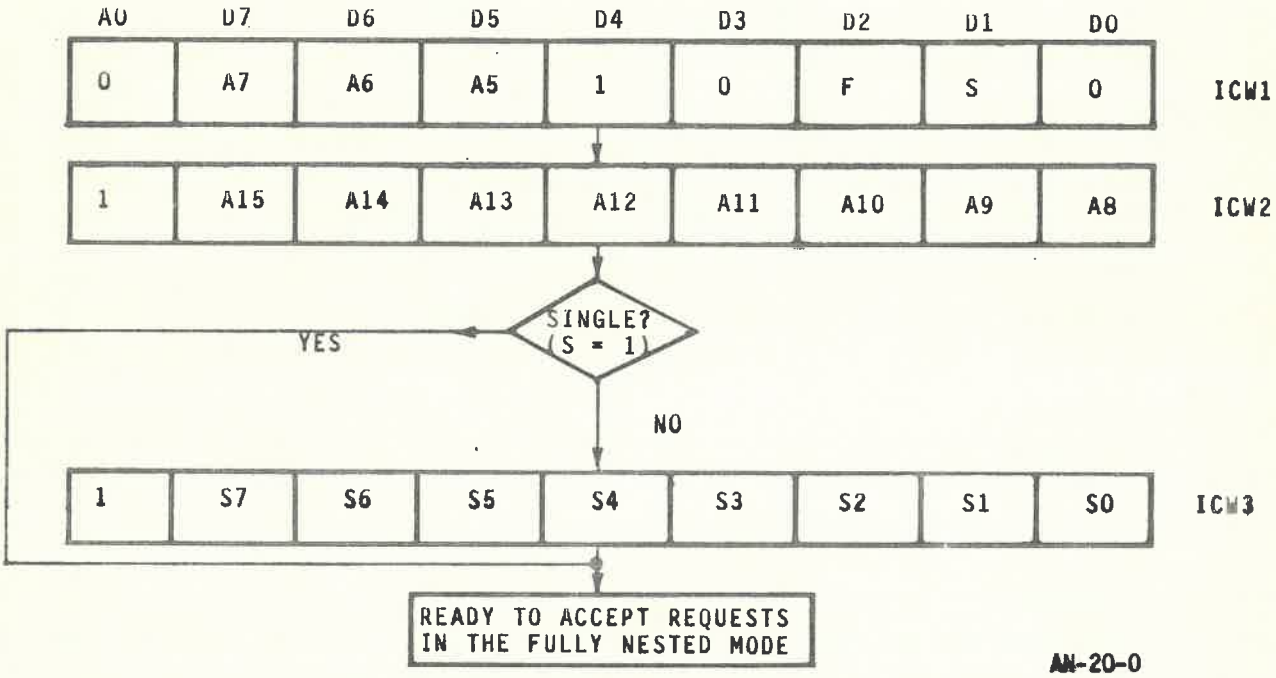


Figure 5-5 8259 Initialization Sequence

Once the CPU has acknowledged an interrupt (INTA/), lower priority interrupt levels remain inhibited even after the original interrupt level is masked. The lower priority interrupts can be enabled by using an End of Interrupt originated by an OCW2 command to reset the ISR bit or by using OCW3 with a special mask mode.

OCW2 - This command provides a means of converting the fully nested mode into modes whose priorities can be changed by software.

The algorithm for the Rotating Priority Mode (Auto Mode), which is also called a Rotate-at-EOI mode, can be used when interrupting devices are considered to be equal in priority, as in the case of communications channels. IR0 is assigned the highest priority; IR7 the lowest. After the interrupt request with the highest priority is serviced, the interrupt request with the next highest priority is serviced, etc. As each peripheral is serviced, it is assigned the lowest priority. The change in priority is illustrated by the following:

Initially

In Service Register Bits

IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
0	0	1	1	0	1	0	0

Lowest ← Priority → Highest

7	6	5	4	3	2	1	0

After Rotation

In Service Register Bits

IS2	IS1	IS0	IS7	IS6	IS5	IS4	IS3
0	0	0	0	0	1	1	0

Lowest ← Priority → Highest

7	6	5	4	3	2	1	0

In the above example, IS2 initially had the highest priority of the three interrupt request lines requesting service. After being serviced, it was rotated to a position of lowest priority and IS4 will be the next in line to be serviced.

The Rotating Priority Mode (Specific Mode) enables the user to set priorities by programming the interrupt Request Level with the lowest priority, using the BCD code (D2, D1 and D0) to call out the IR level number. The next highest IR level is automatically assigned highest priority. If IR3 is called out for the lowest priority, IR4 will have the highest priority. The lowest priority device is thereby selected without affecting the ISR, and independently of the EOI. The type of Rotate, Priority-Rotate or Not-Rotate is determined by bit D7 of OCW2 as shown in Figure 5-6.

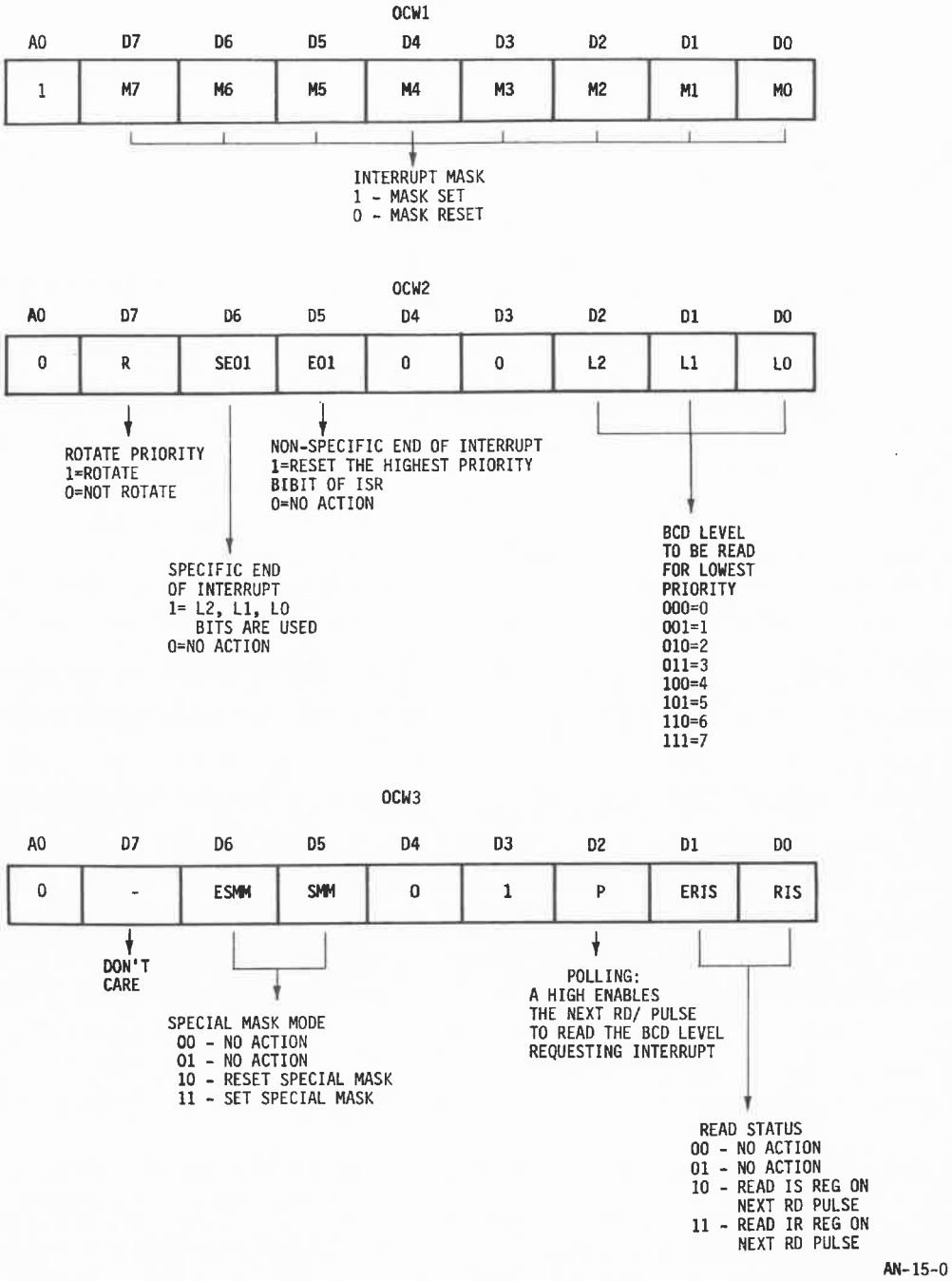


Figure 5-6 8259 Operation Command Word Format

End of Interrupt EOI and SEOI

When a routine has been completed, it issues an End of Interrupt command to reset the IS bit being serviced. Therefore, the 8259 must be able to determine which IS bit is to be reset after receiving an EOI. With the fully nested mode, a general or "non-specific" EOI will result in the resetting of the highest IS bit of those that are set because that bit represents the IR level being serviced. This non-specific EOI should only be used with the fully nested mode. However, when another interrupt mode, such as the rotating mode, is used, the highest IS bit is not necessarily the last level acknowledged and serviced. In this case a specific EOI (SEOI), which includes the BCD code for the IS priority level to be reset must be issued by the CPU. L2, L1, L0 in OCW2 provides the BCD code to specify the IS level to be reset. SEOI and EOI are selected by bits D6 and D5 respectively of OCW2. A Rotate command can be issued while EOI is active for this mode is independent of the type of EOI command.

Note: For any mode other than the fully nested mode, it is desirable to use a specific EOI to avoid confusion as to which ISR bit is to be reset. With the SEOI command, priorities are not rotated after the IRS bit is reset.

Special Function Control Operation-Command Word 3 (OCW3)

OCW3 is used to control the special mask mode (SMM), the polling mode and the reading of 8259 status registers, as shown in the Operation Command Word Summary, Table 5-2.

Special Mask Mode (SMM)

SMM is used to enable lower priority interrupt levels after the level corresponding to the routine has temporarily been masked by an OCW1 command. Then the SMM command can easily be reset by another OCW3 command. Higher priorities are not affected by this command.

The alternative way to enable lower priority interrupt levels would be to reset the ISR bit of the routine being serviced with an EOI command. In that case the lower priority interrupt would remain enabled until another interrupt request was received for the ISR bit of the routine being serviced.

Polled Mode

In this mode the CPU polls the 8259 for the identity of the interrupting device rather than polling individual I/O device as with conventional techniques. All of the previously described priority modes can be used and the same program can use both this polling mode and the vectored interrupt methods.

This mode is also useful if the same routine command is used for several levels because the INTA sequence is avoided, thereby conserving RAM space.

TABLE 5-2 8259 OPERATION COMMAND WORD PROGRAMMING SUMMARY

WORD	A0 D4 D3	VARIABLE	OPERATIONS
OCW1	1	M7-M0	IMR (Interrupt Mask Register). WR/ will load it; status is read with RD/.
OCW2	0 0 0	R SEOI EOI	
		0 0 0	No Action
		0 0 1	Non-specific End of Interrupt.
		0 1 0	No Action
		0 1 1	Specific End of Interrupt. L2, L1, L0 is the BCD level to be reset.
		1 0 0	No Action
		1 0 1	Rotate priority at EOI. (Auto Mode)
		1 1 0	Rotate priority L2,L1,L0 establish bottom priority without Ending of Interrupt.
		1 1 1	Rotate priority at EOI (Specific Mode). L2,L1,L0 establish bottom priority, and the corresponding IS flip-flop is reset.
OCW3	0 1 0	ESMM SMM	
		0 0	Special Mask not affected.
		0 1	Special Mask not affected.
		1 0	Reset Special Mask.
		1 1	Set Special Mask.
		ERIS RIS	
		0 0	No Action
		0 1	No Action
		1 0	Read IR Register Status.
		1 1	Read IS Register Status.

Note: The Z80 INT input must be disabled during:
1. Initialization sequence for all 8259s in the system.
2. Any control command execution.

The polling mode is implemented by setting P=1 (D2) in OWC3 to produce an Interrupt Acknowledge (INTA). This software controlled interrupt acknowledge, like the hardware originated signal, sets the highest priority input. The 8259 then enables the BCD code of the highest level requesting service to be read onto the data bus at the next RD/pulse, which could be originated by an Input command. The word format is:

D7	D6	D5	D4	D3	D2	D1	D0
1	x	x	x	x	W2	W1	W0

where D7=1 if an interrupt occurred and W2-W0 is the BCD code for the highest priority ISR bit set.

To use the polled command, interrupts must be disabled first, either with a DI instruction or by an interrupt occurring. Then the OCW3 command with P=1 is sent to the 8259 using an output command or a WR/pulse.

The next RD/pulse is then treated as an interrupt acknowledge. The software decodes the polled word and branches to the appropriate routine.

The OCW2 command must be written before the RD/pulse each time a poll is taken.

5.4.3 Reading The 8259 Status

OCW3 commands are also used to read the status of the: 1) Interrupt Request Register (IRR), 2) In Service Register, and 3) Interrupt Mask Register. The 8259 remembers which register was last selected for a status read operation so an OCW3 command need not be written before each read operation unless the register to be read has been changed.

When used for a polling operation, the OCW3 must precede each read command. IRR is read by a RD/ pulse that has been preceded by a WR/ pulse and OCW3 when ERIS=1, RIS=0. ISR can be read in a similar manner when both ERIS and RIS=1. IMR is read when RD/ is active and AO=1 even when RD/ is not preceded by WR/.

The polling command overrides the Status Read command when P=1 and ERIS=1.

5.5 INPUT/OUTPUT BLOCK

The I/O block within the System Processor board consists of the following three types of devices:

- Timer (8253)
- Parallel Communication Interface (8255A)
- Serial Communication Interface (8251)

The devices are located on the micro bus within the System Processor board and are not accessible from the MULTIBUS. The specific address assignments for the devices are provided in Table 5-3.

5.5.1 Timer (8253)

The 8253 provides clocks for the two 8251 RS232C interface USARTS and the system interrupt timer on interrupt level 2. Counter 0 provides the interrupt timer. Counter 1 provides the baud clock for USART #1, and Counter 2 provides the baud clock for USART #2.

Functions of the 8253 are completely determined by system software. A set of control words sent out by the CPU initializes each counter with the desired function and quantity information.

Because exclusive addresses are assigned to the count register in each counter, simple I/O procedures are used to program each counter.

The Mode Control Word format for programming the function, loading sequence, and type of counting (binary or BCD) is given in Figure 5-7.

The Mode Control Word is then followed by one or two count register bytes which, with A1 and A0, determine which counter is loaded or read. The gate/trigger function for each mode is given in Table 5-4.

Although counters are 16 bits long and two I/O instructions are required to fully load a register, the read/load bits (RL1, RL0) may specify only one byte (LSB or MSB) in which case only one I/O instruction is required.

Mode 0 - Interrupt On Terminal Count

Counter output is low after the mode is set and remains low while the count is loaded into the count register and the counter counts down. The counter output goes high when the terminal count is reached and remains high until the selected count register is reloaded or the mode is set again. A high gate input enables counting; a low gate input inhibits counting. Reloading a count register during counting restarts the procedure.

Mode 1 - Programmable Retriggerable One-Shot

Following the rising edge of the Gate/Trigger input, output goes low. On the terminal count, output goes high. Loading a new count value while the output is low does not affect the one-shot pulse duration until the succeeding gate/trigger input occurs. Reading the current count also does not affect the one-shot pulse. In this mode, there is no count gate.

TABLE 5-3 DEVICE ASSIGNMENTS

I/O PORT ADDRESS HEX	I/O DEVICE	INPUT FUNCTION	OUTPUT FUNCTION
70 71 72 73 74 75 76 77	Disk Controller, BLC 8222	Status Byte Error Byte --- --- --- --- --- ---	--- IOPB Memory Addr. Low IOPB Memory Addr. High --- --- --- --- RESET
D0-D3	RAM/ROM OFF	Read RAM/ROM OFF Override, and Power Fail Status	SET or RESET RAM/ROM OFF Control
D4-D5	System Bus Override	Read RAM/ROM OFF, Override, and Power Fail Status	Set or Reset Override Control
D6-D7	Memory Map	Read Map Segments	Write Map Segments
D8	INS8259 Interrupt Control (Master)	Read ISR, IRR or current Interrupt Level (based on the contents of OCW3)	Data Bit D4 D3 0 0 Load OCW2 0 1 Load OCW3 1 X Load ICW1
D9		Read Interrupt Mask Register (IMR)	Load OCW1, ICW2, or ICW3 (depending on sequence)
DA	INS8259 Interrupt Control (Master)	Read ISR, IRR or current Interrupt Level (based on the contents of OCW3)	Data Bit D4 D3 0 0 Load OCW2 0 1 Load OCW3 1 X Load OCW1
DB		Read Interrupt Mask Register (IMR)	Load OCW1, ICW2, or ICW3 (depending on sequence)
DC DD DE DF	INS8253 Interval Timer	Read Counter 0 Read Counter 1 Read Counter 2 *NOT USED	Load Counter 0 Load Counter 1 Load Counter 2 Mode Control
E0-E3	* Unassigned		
E4 E5 E6 E7	INS8255 PPI #1 (Printer Interface)	STATUS --- --- ---	--- Control Data & Control INS8255 Control
E8 E9 EA EB	INS8255 PPI #2	Unassigned Unassigned Unassigned ---	Unassigned Unassigned Unassigned INS8255 Control
EC ED EE EF	INS8251 USART #1 INS8251 USART #2 } CRT	Data In Read Status Data In Read Status	Data Out Control Data Out Control } CRT
*These addresses are not available for use by external I/O devices.			

TABLE 5-4 8253 GATE/TRIGGER FUNCTIONS

MODE	SIGNAL STATUS		
	RISING	HIGH	LOW OR GOING LOW
0 - Interrupt on Terminal	----	Enables counting	Disables Counting
1 - Programmable One Shot	1) Initiates counting 2) Resets output after next clock	----	----
2 - Rate Generator	Initiates counting	Enables counting	1) Disables counting 2) Sets output high immediately
3 - Square Wave Rate Generator	Initiates counting	Enables counting	1) Disables counting 2) Sets output high immediately
4 - Software Triggered Strobe	----	Enables counting	Disables counting
5 - Hardware Triggered Strobe	Initiates counting	----	----

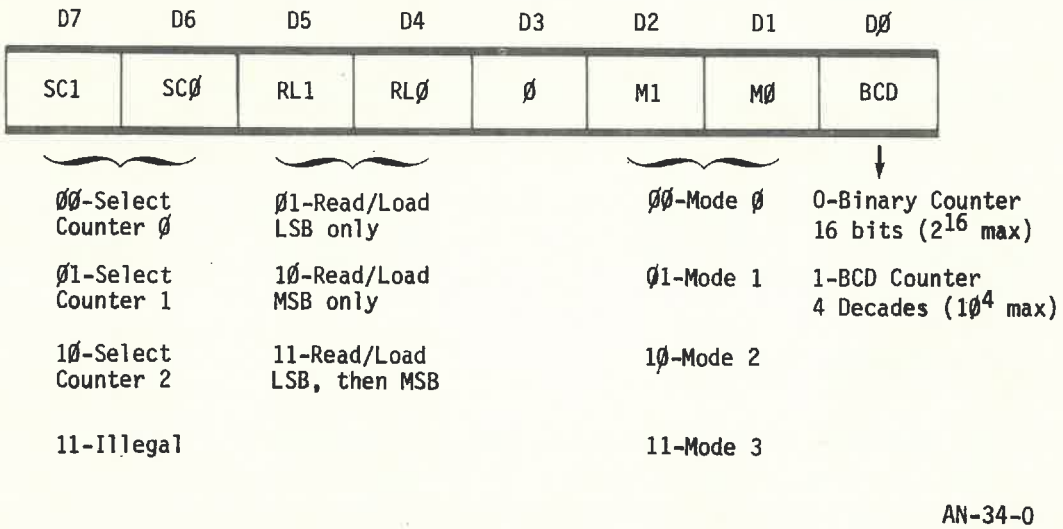


Figure 5-7 8253 Mode Control Word Format

Mode 2 - Rate Generator

This mode uses a divide-by-N counter. When Mode 2 is set, the output is high and remains high until the count register is loaded, at which time the count starts. In this way, software can be used to synchronize the output.

The output goes low for one clock period after the count equals the number of counts in the count register; the period from one output pulse to another equals the number of counts. Reloading the count register between output pulses does not affect the present period but will change the following period.

The gate/reset signal can be used to synchronize the counter. As shown in the timing diagram, a low gate/reset input after the count starts forces the output high and the output will remain high until the gate/reset input goes high. The counter will then start the count over again.

Mode 3 - Square Wave Generator

Mode 3 is similar to Mode 2, except that the count register is loaded after the gate/reset input goes high, and the output remains high for one half of the count and then goes low for the other half (for even counts). If the count is odd, the output will be high for (n+1)/2 counts and low for (n-1)/2 counts. As with Mode 2, when the gate/reset input goes low, output goes high and stays high. When the gate/reset input goes high, the count begins at the beginning of the next clock cycle. If reloaded, the counters reflect the new value immediately after the output of the current count changes.

Mode 4 - Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

Mode 5 - Hardware Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

8253 Timer Operation Summary

Basic Programming Format Rules

1. Mode control word first
2. Count register bytes - sequence and number of bytes based on RL1, RL0
3. Count register bytes need not follow the mode control word directly
4. Mode control words can be in any sequence (0, 1, 2 or 1, 2, 0, etc.)

The following steps are used in programming the desired time configuration:

1. Output a mode control word to the 8253 Control Register using port DF (Hex) in which WR/=0 CS/=0, A0=1, A1=1.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	0	M1	M0	BCD

2. Initialize the counter selected by the mode control word with the required number of count register bytes (LSB and/or MSB).

	Address A_1	A_0
Mode Control Word	1	1 (DF)
Counter 0	0	0 (DC)
Counter 1	0	1 (DD)
Counter 2	1	0 (DE)

Flexible Programming Format Example*

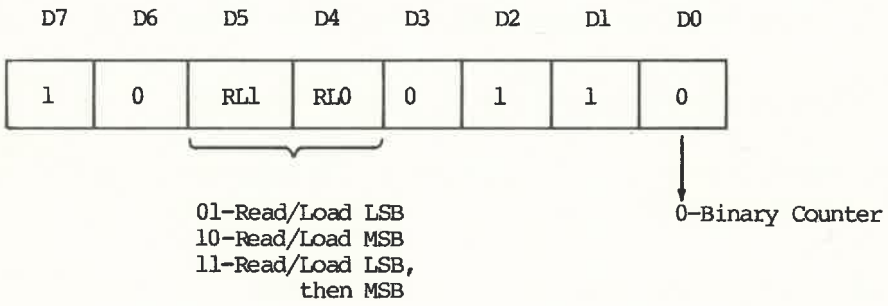
STEP

1. Mode Control Word, Counter 2
2. Counter Register Byte, Counter 2, LSB
3. Counter Register Byte, Counter 2, MSB
4. Mode Control Word, Counter 0
5. Mode Control Word, Counter 1
6. Count Register Byte, Counter 1, LSB
7. Count Register Byte, Counter 0, LSB
8. Count Register Byte, Counter 0, MSB
9. Count Register Byte, Counter 1, MSB

*This example is used only to show that mode control words and count register bytes can be used in a variety of sequences because of the availablity of addresses for each. Limitations are that the mode control word for a particular counter must be programmed before the count register bytes are programmed for that counter, and the sequence and number of bytes is dictated by RL1, RL2 in the mode control word.

Programming Counters 1 and 2

To use counters 1 and 2 to generate the baud rate clocks for the Serial I/O, the counters must be programmed for Mode 3 as square wave rate generators and the primary binary value must be loaded into the counters to produce the desired output frequency (See Table 5-5). The Baud Rate Clock Control Word for Counters 1 and 2 is as follows:



5.5.2 Parallel Ports (8255A)

Two parallel I/O port connections are provided on the System Processor board. Each port provides 24 programmable I/O lines which are controlled through an 8255A (Parallel Communications Interface Controller). One port is configured and dedicated to provide the Centronics printer interface and the other port is unassigned.

The 8255A which is assigned to I/O port addresses E4 through E7 Hex is dedicated to the printer interface. Figure 5-8 shows the input/output assignment and bit maps for this port. To properly configure the 8255A for this usage, a control byte of 90 Hex is written by the Z80A processor to output I/O address E7 Hex. This configures the port to Mode 0 operation with port A as input and ports B and C as output ports. The second 8255A, which is unassignal, occupies I/O addresses E8 through EB Hex.

The remaining paragraphs of this subsection provide programming reference information for the 8255A peripheral controller device.

Data is routed to or from the 8255A upon the execution of either an OUT or an IN instruction, respectively, by the Z80A. Control words and status information are also transferred via OUT or IN instructions.

TABLE 5-5 BAUD RATE FACTORS FOR COMMON COMMUNICATION FREQUENCIES

BAUD RATE CLK FREQUENCIES (KHz), SOFTWARE-SELECTABLE	BAUD RATE FACTOR (hex)		BAUD RATE (Hz)		
			SYNCHRONOUS	ASYNCHRONOUS	
	MSB	LSB		-16	-64
153.6	00	07	—	9600	2400
76.8	00	0E	—	4800	1200
38.4	00	1C	38400	2400	600
19.2	00	38	19200	1200	300
9.6	00	70	9600	600	150
4.8	00	E0	4800	300	75
2.4	01	C0	2400	150	-
1.76	02	63	1760	110	-

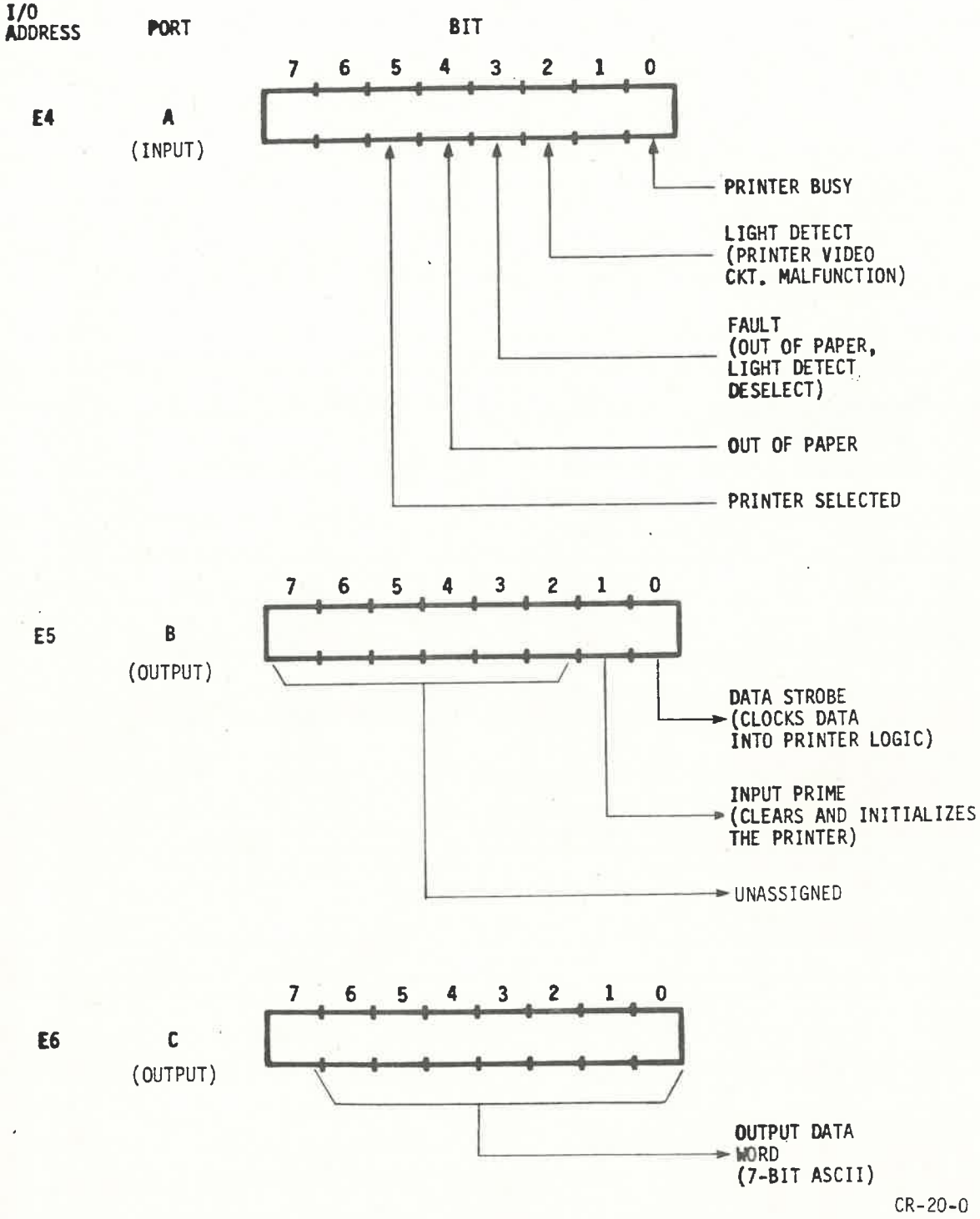


Figure 5-8 Bit Map of 8255 Port Used for Centronics Printer

The read/write control logic supervises all of the internal and external transfers of data, control words, and status information. The logic is enabled by a low-level chip select (CS/) input, which is decoded from the processor address bus when the proper I/O port address is present. When enabled, the read/write control logic accepts either a low-level read (RD/) or low-level write (WR/) input from the processor control bus, and accepts port select inputs (A_0 and A_1) from the address bus. The read/write control logic then issues commands that control the selection of one of the three ports or the control word register as indicated in Table 5-6. A high-level system reset input to the control logic clears all the internal registers and sets all ports to the input mode.

When the 8-bit control word register is selected by the read/write control logic, the register accepts control words from the CPU (via the data bus buffer and internal data bus). The control circuits then supply command outputs that determine the functional configuration of the associated ports.

Three 8-bit ports (A, B and C) are contained in the 8255A. System software uses a Mode Definition Control Word (see Figure 5-9) as the second byte of OUT Instruction(s) to program the functional configuration of ports A through C. Port A comprises one 8-bit output and input latch/buffer. Port B comprises one data input/output latch/buffer. Port C comprises one 8-bit data output latch/buffer or one 8-bit data input buffer. This port can be split into two 4-bit ports under mode control. Each of these 4-bit ports contains a 4-bit latch that can be used for control and status signals in conjunction with ports A and B.

The 8255A has three basic modes of operation that can be selected by system software. In the first mode (Mode 0), the 8255A provides simple input and output operations for the three 8-bit ports. Data is simply written to or read from a specified port (port A, B or C) in this mode without the use of handshaking signals. Output data is latched but input data is not.

In the second mode (Mode 1), the 8255A enables the transfer of input/output data to or from a specified 8-bit port (port A or B) in conjunction with strobes or handshaking signals with the peripheral device. Ports A and B use the lines of Port C in this mode to generate or accept the handshaking signals with the peripheral device.

Basic Configuration - Mode One

Mode One provides strobed input/latched output (handshaking) operation. Data flow takes place on the lines of Port A and B. Port C provides the handshaking signals. The input/output control signals are:

TABLE 5-6 8255A CONTROL LOGIC

CS	A1	A0	RD	WR	OPERATION SELECTED
0	0	0	0	0	Data read from Port A
0	0	1	0	1	Data read from Port B
0	1	0	0	1	Data read from Port C
0	0	0	1	0	Data written into Port A
0	0	1	1	0	Data written into Port B
1	1	0	1	0	Data written into Port C
0	1	1	1	0	Control word written into Control Word Register
1	X	X	X	X	Device not selected

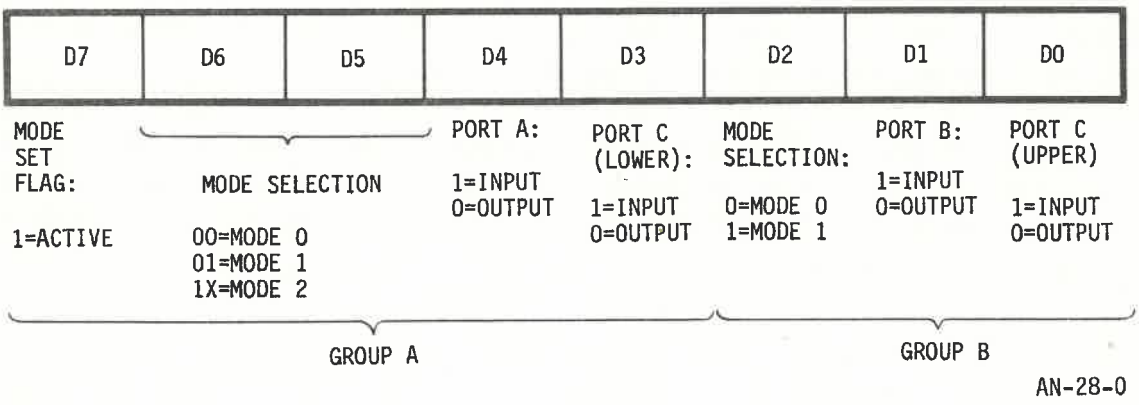


Figure 5-9 8255 Mode Definition Control Word Format

Mnemonic	Meaning	Definition
STB	Strobe Input	Loads data to an input latch.
IBF	Input buffer Full	When a logic one (high) indicates that a data byte has been loaded into the input buffer. IBF is set by STB input being low and reset by RD when the data byte has been retrieved by the CPU.
INTR	Interrupt Request	A signal to the CPU indicating that service is needed. If interrupt is enabled (INTE=1 and IBF=1), INTR is set by STB=1. It is reset by RD. The interrupt enable for Port A (INTE A) is controlled by the state of Port C bit 4 (PC_4). The interrupt enable for Port B (INTE B) is derived from PC_2. A "1" enables an interrupt, a "0" disables it.
OBF	Output Buffer Full	When true (logic zero) indicates that data has been written to the specified port by the CPU. Set by WR and reset by ACK.
ACK	Input Acknowledge	Acknowledges that a data byte has been received by the specified Port A or Port B.

Basic Configurations - Mode Two

In Mode 2, Port A becomes a bidirectional data bus for parallel data exchange with peripheral devices. Port B can operate in Mode 0 or Mode 1 configuration only (unidirectional bus). Port C provides 5 control and status bits for use with Port A. The input/output control signals are:

Output	Meaning	Definition (Applies to Port A Only)
INTR	Interrupt Request	Interrupt line to the CPU for I/O operations. Uses PC_3.
OBF	Output Buffer Full	A low (logic zero) signals that data has been sent to Port A by the CPU.
ACK	Acknowledge	A low enables data to be sent from the Tri-state output buffer of Port A.
INTE 1	Interrupt Enable	PC_6 controls the interrupt enable (INTE1) associated with OBF.

Input	Meaning	Definition (Applies to Port A Only)
INTR	Interrupt Request	Same as output.
STB	Strobed Input	Loads data into the input latch.
IBF	Input Buffer Full	Signifies that data has been loaded into the input latch.
INTE 2	Interrupt Enable	PC_4 controls the interrupt enable (INTE2) associated with IBF.

In Mode 2, the 8255A enables communications with a peripheral device or structure via one bidirectional 8-bit bus port (Port A). Handshaking signals are provided over the lines of Port C in this mode to maintain proper bus flow discipline.

The mode for Port C (upper and lower bits) depends in part on the modes selected for Ports A and B. Ports A and B can be programmed to operate simultaneously in different modes, i.e., Port A can be in Mode 0 while Port B is in Mode 1.

In Modes 1 or 2, any of the Port C lines not used for handshaking can be accessed using the bit set/reset feature.

Figures 5-10 and 5-11 show the status information that is provided at Port C for Modes 1 and 2, respectively. A normal read operation is executed to read this status information.

Mode 0 input is considered to be the basic mode and is the mode in which the 8255A is placed by a RESET operation. A mode change resets all of the output registers except for OBF/, in Modes 1 and 2.

The CPU can set or reset any of the bits of Port C by writing a Bit Set/Reset control word (Figure 5-12). This feature greatly simplifies control of input/output operations for the System Processor. For operation in Mode 1 or Mode 2, control signals are available to generate an interrupt request to the CPU. These originate from Port C and are configured by the Bit Set/Reset control word. Generally, if a control bit associated with an interrupt is set, then the interrupt enable to the 8255A is set. If the associated bit is reset, then the interrupt enable is disabled. Mode selection and RESET will disable all interrupt masks.

Table 5-7 summarizes the 8255A mode operation.

5.5.3 Serial Ports 8251

The complete functional definition of the two 8251 RS232C interface USARTs are programmed by the system software. Before the actual start of data transmission or reception, the 8251 must be loaded with a set of control words (Mode Instruction and Command Instruction) that are generated by the Z80A. The mode instruction word defines the general operational characteristics of the 8251. This control word must immediately follow a reset operation (internal or external).

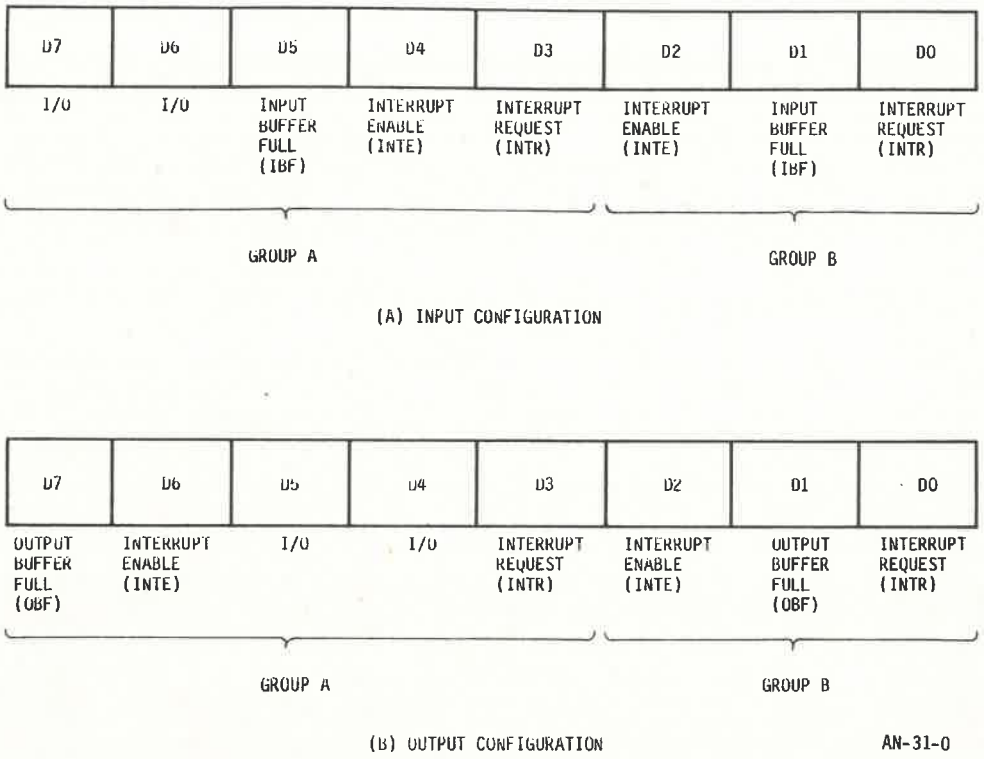


Figure 5-10 8255A Mode One Status Word Format

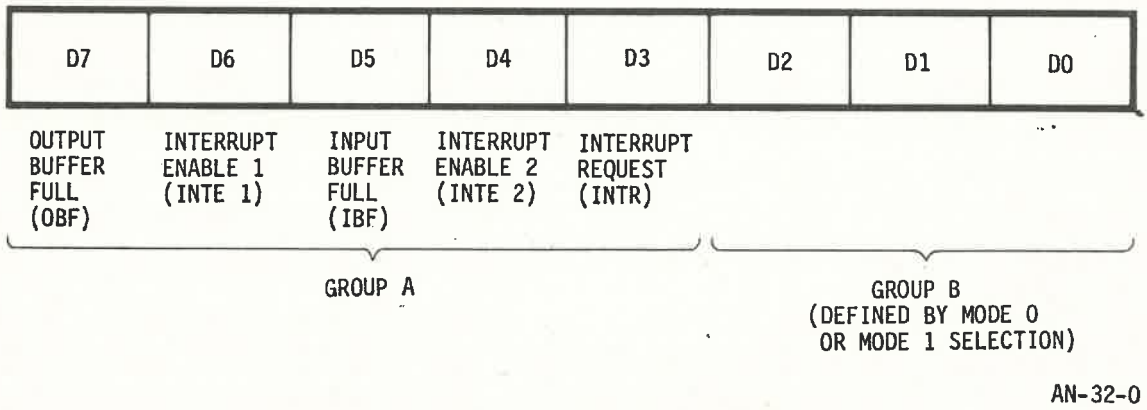


Figure 5-11 8255A Mode Two Status Word Format

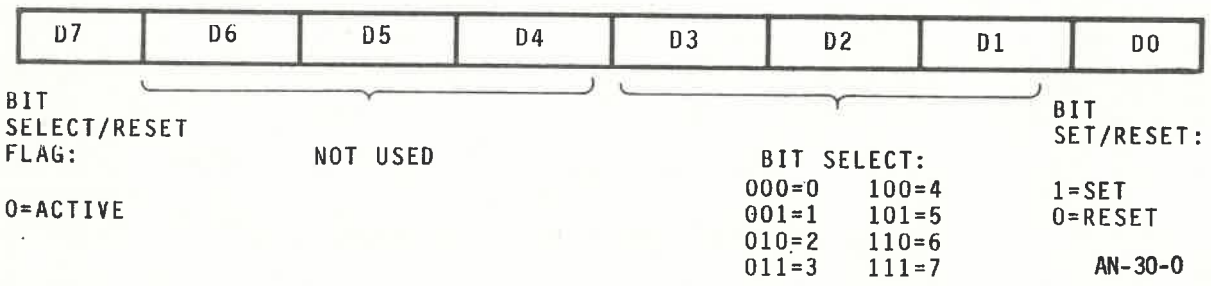


Figure 5-12 8255A Set/Reset Control Word Format

TABLE 5-7 8255A MODE OPERATION SUMMARY

This table shows the application of Port C bits for all Port A and Port B mode combinations.

		<--INPUT TO PPI					--> OUTPUT FROM PPI				
		PORT-MODE	PORT-MODE		PORT-MODE		PORT-MODE		PORT-MODE	PORT-MODE	
		A-0 B-0	A-1 B-0		A-0 B-1		A-1 B-1		A-2 B-0	A-2 B-1	
	PORT A PA0-7	BASIC I/O	INPUT STROBED	OUTPUT LATCHED	BASIC I/O	BASIC I/O	INPUT STROBED	OUTPUT LATCHED	BIDIRECT.	BIDIRECT.	Port A
4-Bit* Port C	PC7	I/O	I/O	OBFA-->	I/O	I/O	I/O	OBFA-->	OBFA-->	OBFA-->	OBFA-->
	PC6	I/O	I/O	ACKA<--	I/O	I/O	I/O	ACKA<--	ACKA<--	ACKA<--	ACKA<--
	PC5	I/O	IBFA-->	I/O	I/O	I/O	IBFA-->	I/O	IBFA-->	IBFA-->	IBFA-->
	PC4	I/O	STBA<--	I/O	I/O	I/O	STBA<--	I/O	STBA<--	STBA<--	STBA<--
	PC3	I/O	INTRA-->	INTRA-->	I/O	I/O	INTRA-->	INTRA-->	INTRA-->	INTRA-->	INTRA-->
4-Bit* Port C	PC2	I/O	I/O	I/O	STBB<--	ACKB<--	STBB<--	ACKB<--	I/O	STBB<--	ACKB<--
	PC1	I/O	I/O	I/O	IBFB-->	$\overline{\text{OBFB}}$-->	IBFB-->	$\overline{\text{OBFB}}$-->	I/O	IBFB-->	$\overline{\text{OBFB}}$-->
	PC0	I/O	I/O	I/O	INTRB-->	INTRB-->	INTRB-->	INTRB-->	I/O	INTRB-->	INTRB-->
	Port B PB0-7	Basic I/O	Basic I/O	Basic I/O	Input Strobed	Output Latched	Input Strobed	Output Latched	Basic I/O	Input Strobed	Output Latched

Port C Control and Status Bits Associated With Port A

Port C Control and Status Bits Associated With Port B

Port B

*When not required to provide control and status bits for Port A and B, Port C can be split into two 4-bit I/O ports. All lines for each 4-bit port must provide the same function - either input or output.

After the mode instruction word is written into the 8251, synchronous or asynchronous operation has been defined. Synchronous operation requires the insertion of sync characters prior to command instructions, as shown in Figure 5-13. This differs from asynchronous operation in which all control words, written into the 8251 after the mode instruction word, load the command instruction words.

The command instruction word defines a status word that is used to control the actual operation of the 8251. Command instructions may be written into the 8251 at any time in the data block during the operation of the device. To return to the mode instruction word format, bit D_6 of the command automatically causes the 8251 to treat the next received character as the new mode instruction word.

Mode Instruction Format

Figure 5-14 shows the mode instruction format for asynchronous operation. Figure 5-15 shows the asynchronous mode data format. Figure 5-16 shows the mode instruction word for synchronous operation. Figure 5-17 shows the synchronous mode data format.

Command Instruction Format

The command mode instruction establishes the operating mode and parameters for the 8251. The command instruction controls the actual operation of the 8251. Figure 5-18 defines each bit of the command instruction.

5.6 BUS INTERFACE BLOCK

The Bus Interface logic makes it possible for the System Processor to access and control system memory and I/O devices such as the DMA controller. This interface consists of an H8218 Bus Controller, an Override Flip-Flop, Bus drivers/receivers, Bus Clock and Common Clock signals.

5.6.1 Bus Controller

The Bus Controller, operating synchronously with the Bus Clock (BCLK/), determines which master will use the system bus when there are a number of bus requests. If the System Processor gains control of the bus, the Bus Controller enables the required memory and I/O command signals, gates the address onto the address lines and data on or off the bus at appropriate times. The required set-up and hold time relationships between the address/data lines and control signals are developed by an external RC network connected to the Bus Controller's Delay-Adjust (DLYADJ/) input.

A timing reference for the controller's bus arbitration logic is provided by the negative-going edge of the Bus Clock signal (BCLK/). This signal can be supplied to pin P1-13 from an external source or it can be generated on the System Processor board by connecting jumper group W25 pin 3 and 4.

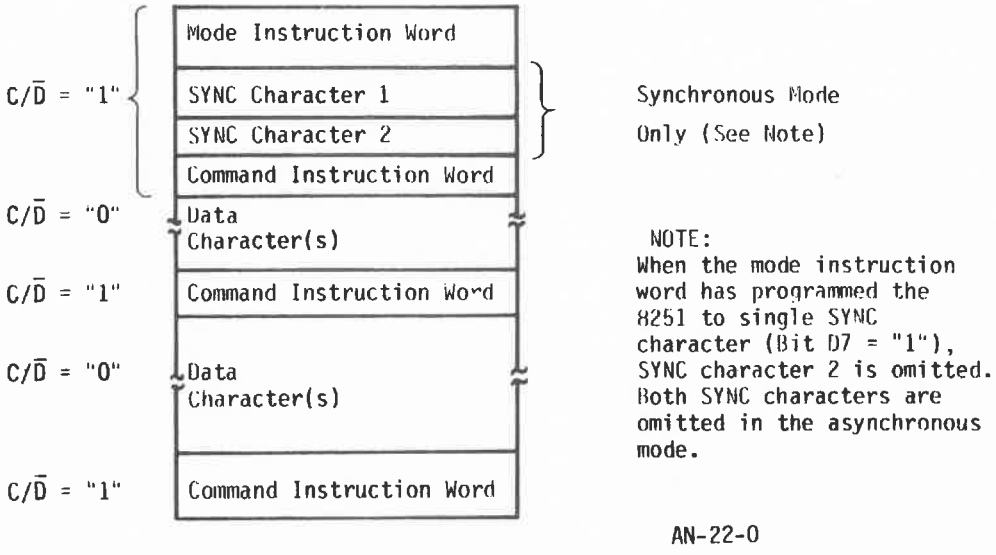

Mode Instruction Word
C/D̄ = "1"
SYNC Character 1
SYNC Character 2
Command Instruction Word
C/D̄ = "0"
Data Character(s)
C/D̄ = "1"
Command Instruction Word
C/D̄ = "0"
Data Character(s)
C/D̄ = "1"
Command Instruction Word
Synchronous Mode Only (See Note)
NOTE:
When the mode instruction word has programmed the 8251 to single SYNC character (Bit D7 = "1"), SYNC character 2 is omitted. Both SYNC characters are omitted in the asynchronous mode.
AN-22-0

Figure 5-13 Typical 8251 Data Transfer

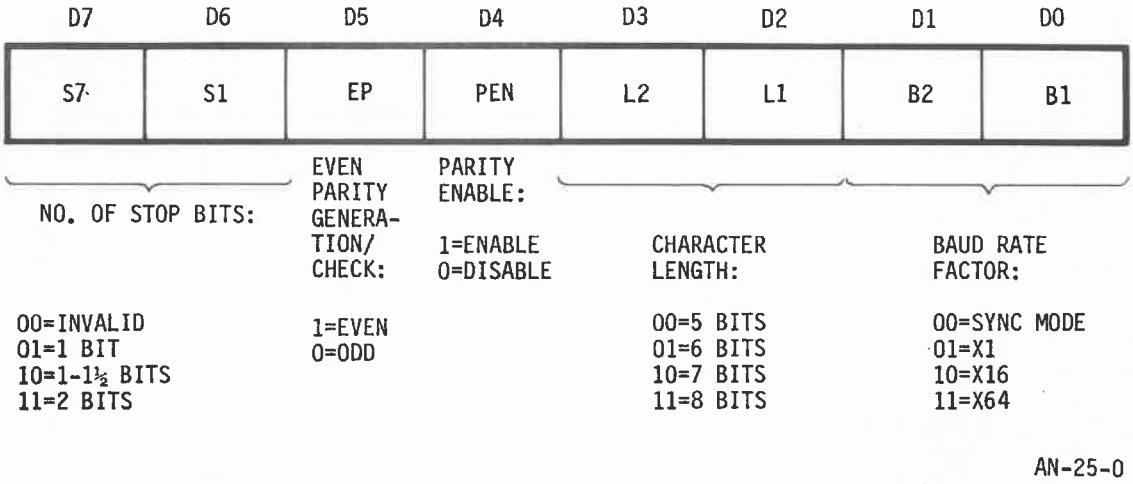


Figure 5-14 8251 Mode Instruction Word Format for Asynchronous Operation

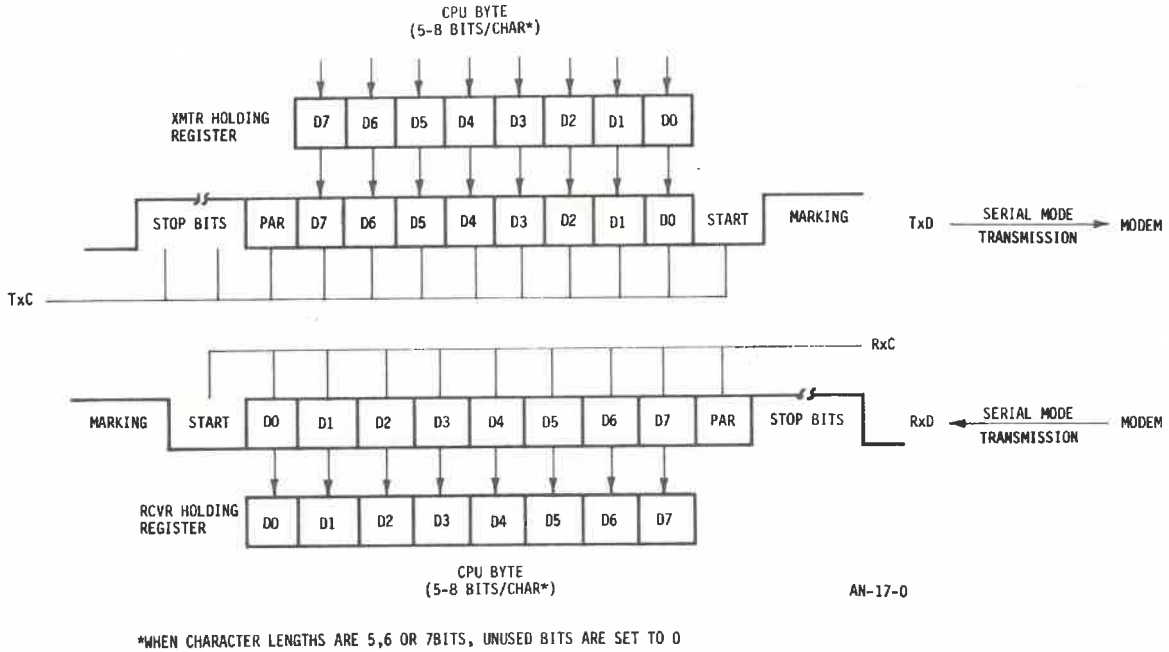


Figure 5-15 8251 Asynchronous Mode Data Byte Configuration

D7	D6	D5	D4	D3	D2	D1	D0
SCS	ESD	EP	PEN	L2	L1	0	0
SINGLE CHAR. SYNC: 1=SINGLE SYNC CHAR. 0=DOUB. SYNC CHAR.	EXTERNAL SYNC DETECT: 1=SYNDET IS AN INPUT 0=SYNDET IS AN OUTPUT	EVEN PARITY GENERATION/ CHECK: 1=EVEN 0=ODD	PARITY ENABLE: 1=ENABLE 0=DISABLE	CHARACTER LENGTH 00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS		SYNC MODE: 00	

AN-24-0

Figure 5-16 8251 Mode Instruction Word Format for Synchronous Operation

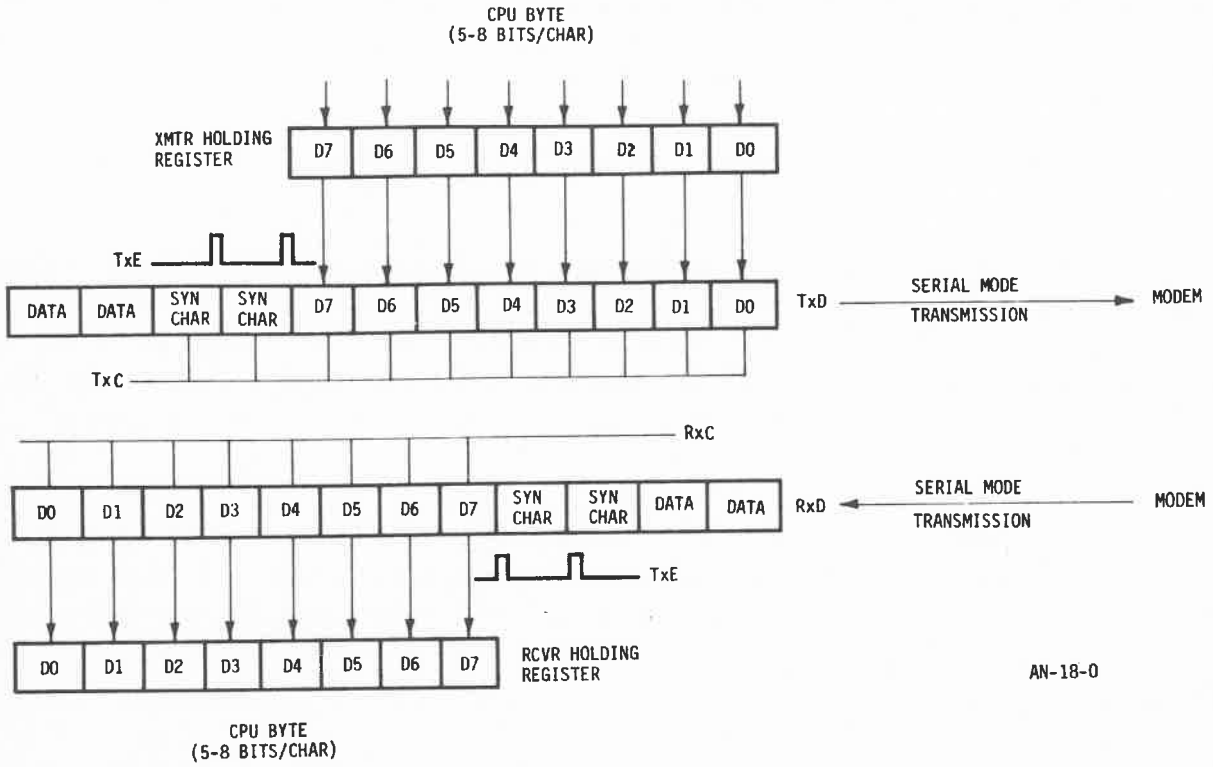


Figure 5-17 8251 Synchronous Mode Daya Byte Configuration

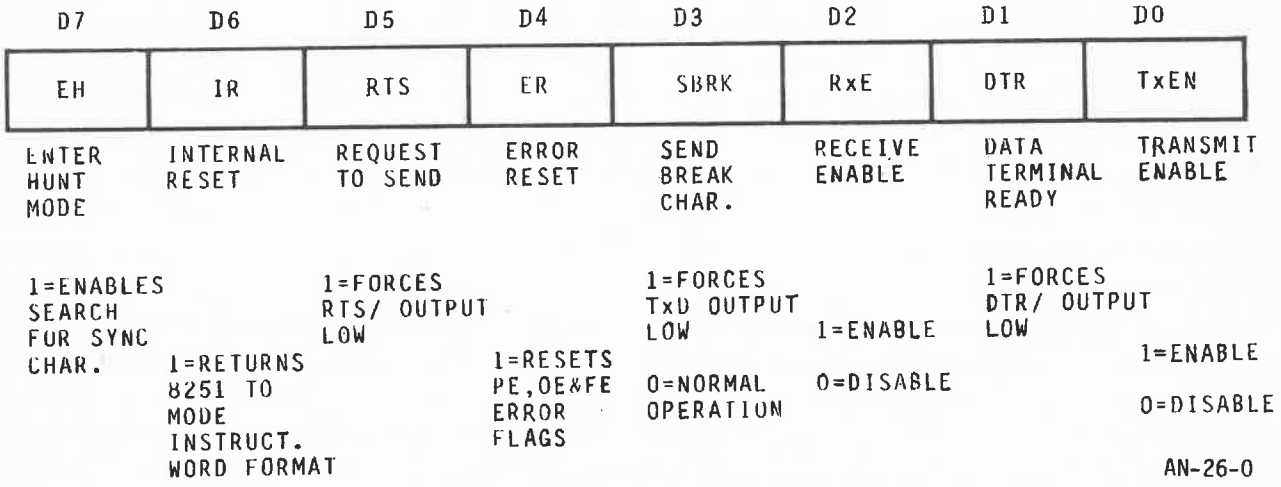


Figure 5-18 8251 Command Instruction Word Format

A 9.216 MHz clock, generated from an on-board oscillator for use by the system DMA controller boards, is provided on the Common Clock (CCLK/) line (P1-31), Bus Clock (BCLK/) line (P1-13), and the Bus Controller by connecting jumper group W25 pairs 1-2 and 3-4.

5.6.2 Bus Control

After bus request is strobed in by BCLK/, the Bus Controller generates a Bus Request (BREQ/) signal on P1-18 and drives the Bus Priority Out signal (BPRO/) high on P1-16 if jumper group W26 pin 1 and 2 are connected (Factory installed jumper). The BPRO/ signal is used in the system serial priority scheme to permit lower priority masters to gain control of the system bus when a master with higher priority is idle. This signal is fed to the Bus Priority In (BPRN/) input of the next lower priority master.

Common Bus Request, CBRQ, is implemented. It is activated whenever a master wants control of the bus but doesn't have control yet. This will provide for automatic override when no other master is requesting the MULTIBUS. This feature is provided by connecting jumper group W27 pin 2 to pin 3. Since the other master board within the system does not utilize this signal, it is not used in the present system operation.

With the System Processor board controlling the bus, the BPRN/ input is low. The Bus Controller then provides a BUSY/ signal (P1-17) to prevent another master from taking control of the bus, and also enables Address and Data Enable (ADEN/) outputs. ADEN/ enables the bus drivers which drive the system address (ADR0/-ADR13/) and data busses (DAT0/-DAT7) and also the Bus Acknowledge gate. The Bus Acknowledge gate is used to gate external acknowledge signal XACK/ to the CPU's WAIT/ pin.

After the ADEN/ signal is generated, the Bus controller starts an internal sequence which generates the memory and I/O read/write control output (MRDC/, MWTC/, IORC/ or IOWC/), depending on the command request signal (MEMR/, MWT/, IOR/ or IOWT/) received from the CPU.

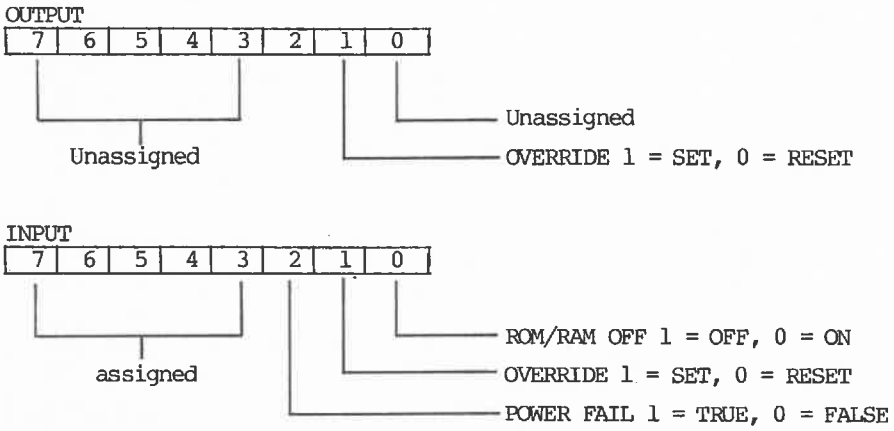
The Bus Controller also generates outputs during the external access operations - one of which, RDD (Read Data), is driven high whenever a Read command request input is active. RDD controls the direction of the buffers which drive the System Data Bus (DAT0/-DAT7/). It is always low, indicating a write mode, until an active Read Command (MEMR/ or IOR/) is received. It then returns to a low state after the read control output (MRDC/ or IORC/) goes inactive.

Unless the System Processor is in the middle of a transfer or has its override flip-flop set, it will lose control of the system bus whenever its BPRN/ input goes high and the original bus request input (MBRQ/ or IORQ/) becomes inactive.

The Bus Controller is initialized when its INIT/ input goes low.

5.6.3 Override

This control logic is set and reset through I/O writes. The OVERRIDE occupies I/O address D4 and D5. The bit assignment is as indicated below:


OUTPUT
7 6 5 4 3 2 1 0
Unassigned
Unassigned
OVERRIDE 1 = SET, 0 = RESET
INPUT
7 6 5 4 3 2 1 0
ROM/RAM OFF 1 = OFF, 0 = ON
assigned
OVERRIDE 1 = SET, 0 = RESET
POWER FAIL 1 = TRUE, 0 = FALSE

Upon power-up or backplane initialization, OVERRIDE is reset. This enables normal bus master exchange. OVERRIDE set enables the override input to the system processor bus controller and locks out all other bus masters once the processor acquires the bus.

The POWER FAIL input is provided through connector P2 for other system configuration than the 6600 System and is always low in the present use.

NOTE: Override is used by the system software to increase system performance and therefore should be properly set and reset within driver routines which control any DMA or Bus MASTER devices which are added to the system. Refer to the System Software Reference Manual on specifics, within the BIOS, on control of the OVERRIDE flip-flop.

5.6.4 Priority Resolution

The System Processor uses the 8218 System Bus Controller as an interface to the system bus. Although the 8218 has a role in resolving bus contention, it is not a bus arbitrator. It merely receives and acts upon the result of an arbitration of requests for the system bus by various masters. The 6600 System uses Serial Priority Resolution which is established by the physical position of the cards in the card cage which arbitrates access to the bus. Figure 5-19 shows the equivalent circuit of a serial priority scheme for three bus masters (the existing system contains two since the 64K RAM board is not a master).

In the illustration, bus master board A has the highest priority; therefore, its bus request should be permanently enabled by grounding ABPRN/ (A Bus Priority Request In). If master A does not request the bus, ABREQ/ is high. ABPRO/ then goes low, granting master B the use of the bus if its bus request is active. If master B does not require the bus, the BPRO/ output to master C goes low, enabling master C to use the bus.

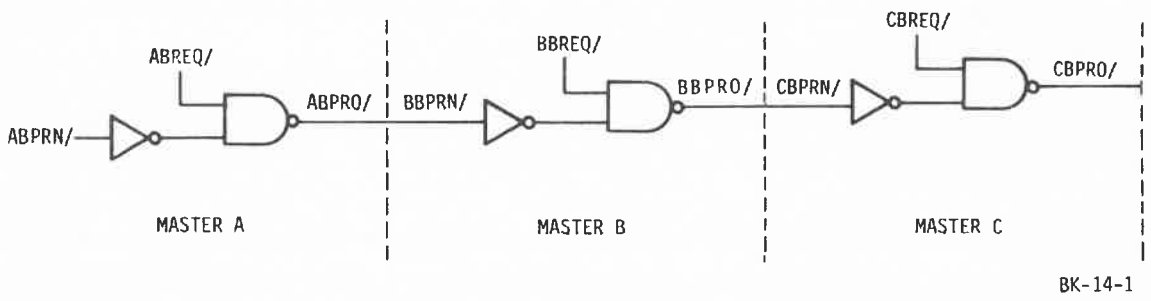


Figure 5-19 Equivalent Circuit for Serial Priority Resolution

If no master requires the system, the BPRN/ inputs to all masters are true. Now suppose that after the next falling edge of BCLK/, bus requests of all three masters go true. Then, before BCLK/ falls again, the serial chain must be able to inform the lower masters (masters B & C) that master A requests the Bus. For master A to obtain control of the system bus, the propagation delay from its bus request to the BPRN/ input of master C, including setup time, is less than one BLCK/.

5.7 RESET AND POWER UP

When power is first applied to the Z80A, the contents of its program counter, stack pointer and other working registers are unknown. To provide a known starting point, a RESET signal is generated until an RC network is sufficiently charged to provide assurance that DC voltages are within specified limits. This signal is applied to the RESET/ input line of the Z80A CPU (Pin 26), resetting the processor's internal program counter to memory location 0000(Hex).

Although the Reset clears the ROM/RAM OFF control flip-flop, it does not affect status flags or any processor working registers - accumulator, registers or stack pointer. Consequently, the contents of these registers remain indeterminate until initialized by a program.

5.8 Z80A INSTRUCTION SET

This section briefly describes the Z80A instruction set, addressing modes and flag operation.

The eight basic Z80A instruction types are:

- Load
- Block Transfer
- Arithmetic and Logic
- Rotate and Shift
- Bit Manipulation
- Jump, Call and Return
- Input/Output
- CPU Control

5.8.1 Introduction To Instruction Types

Load Instructions

The load instructions move data internally between CPU registers and external memory. All of these instructions must specify a source location from which the data is to be moved and a destination location. The source location is not altered by a load instruction. Examples of load group instructions include moves between any of the general purpose registers such as move the data to Register B from Register C. This group also includes load immediate to any CPU register or to any external memory location. Other types of load instructions allow transfer between CPU registers and memory locations. The exchange instructions can trade the contents of two registers.

Block Transfer Instructions

A unique set of block transfer instructions is provided in the Z80A. With a single instruction a block of memory of any size up to 64K can be moved to any other location in memory. This set of block moves is extremely valuable when large strings of data must be processed. The Z80A block search instructions are also valuable for this type of processing. With a single instruction, a block of external memory of any desired length up to 64K can be searched for any 8-bit character. Once the character is found or the end of the block is reached, the instruction automatically terminates. Both the block transfer and the block search instructions can be interrupted during their execution so as to not occupy the CPU for long periods of time.

Arithmetic and Logical Instructions

The arithmetic and logical instructions operate on data stored in the accumulator and other general purpose CPU registers or external memory locations. The results of the operations are placed in the accumulator and the appropriate flags are set according to the result of the operation. An example of an arithmetic operation is adding the accumulator to the contents of an external memory location. The results of the addition are placed in the accumulator. This group also includes 16-bit addition and subtraction between 16-bit CPU registers.

Rotate and Shift Instructions

The rotate and shift group allows any register or any memory location to be rotated right or left with or without carry either arithmetic or logical. Also, a digit in the accumulator can be rotated right or left with two digits in any memory location.

Bit Manipulation Instructions

The bit manipulation instructions allow any bit in the accumulator, any general purpose register or any external memory location to be set, reset or tested with single instruction. For example, the most significant bit of register H can be reset. This group is especially useful in control applications and for controlling software flags in general purpose programming.

Jump, Call and Return Instruction

The jump, call and return instructions are used to transfer control between various locations in the user's program. The group uses several different techniques for obtaining the new program counter address from specific external memory locations. A unique type of call is the restart instruction. This instruction actually contains the new address as a part of the 8-bit OP code. This is possible since only 8 separate addresses located in page zero of the external memory can be specified. Program jumps may also be achieved by loading register HL, IX or IY directly into the PC, thus allowing the jump address to be a complex function of the routine being executed.

Input/Output Instructions

The input/output group of instructions in the Z80A allow for a wide range of transfers between external memory locations or the general purpose CPU registers, and the external I/O devices. In each case, the port number is provided on the lower 8-bits of the address bus during any I/O transaction. One instruction allows this port number to be specified by the second byte of the instruction while other Z80A instructions allow it to be specified as the content of the C register. One major advantage of using the C register as a pointer to the I/O device is that it allows different I/O ports to share common software driver routines. This is not possible when the address is part of the OP code if the routines are stored in ROM. Another feature of these input instructions is that they set the flag register automatically so that additional operations are not required to determine the state of the input data (for example its' parity). The Z80A CPU includes single instructions that can move blocks of data (up to 256 bytes) automatically to or from any I/O port directly to any memory location. In conjunction with the dual set of general purpose registers, these instructions provide for fast I/O block transfer rates.

CPU Control Instructions

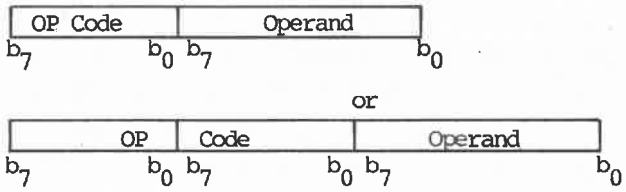
Finally, the basic CPU control instructions allow various options and modes. This group includes instruction such as setting or resetting the interrupt enable flip-flop or setting the mode of interrupt response.

5.8.2 Addressing Modes

Most of the Z80A instructions operate on data stored in internal CPU registers, external memory or in the I/O ports. Addressing refers to how the address of this data is generated in each instruction. This section gives a brief summary of the types of addressing used in the Z80A while subsequent sections detail the type of addressing available for each instruction group.

Immediate

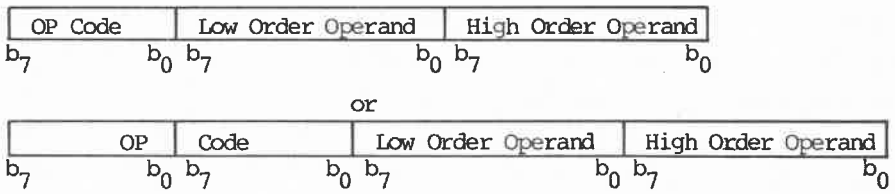
In this mode of addressing the byte following the OP code in memory contains the actual operand.



An example of this type of instruction would be to load the accumulator with a constant, where the constant is the byte immediately following the OP code.

Immediate Extended

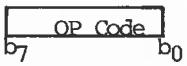
This mode is merely an extension of immediate addressing in that the two bytes following the OP codes are the operand.



An example of this type of instruction would be to load the HL register pair (16-bit register) with 16 bits (2 bytes) of data.

Modified Page Zero Addressing

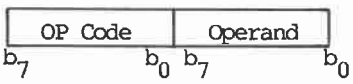
The Z80A has a special single byte CALL instruction to any of 8 locations in page zero of memory. This instruction (which is referred to as a restart) sets the PC to an effective address in page zero. This instruction allows a single byte to specify a complete 16-bit address where commonly called subroutines are located, thus saving memory space.



one byte
Effective address is $(00b_5\ b_4b_3000)$

Relative Addressing

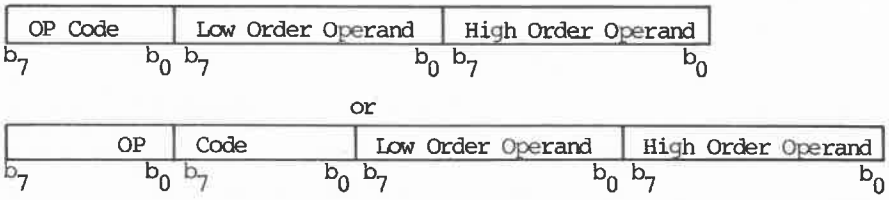
Relative addressing uses one byte of data following the OP code to specify a displacement from the existing program to which a program jump can occur. This displacement is a signed two's complement number that is added to the address of the OP code of the following instruction.



Relative addressing allows jumps to other locations while only requiring two bytes of memory space. For most programs, relative jumps are by far the most prevalent type of jump due to the proximity of related program segments. Thus, these instructions can significantly reduce memory space requirements. The signed displacement can range between +127 and -128 from A + 2. This allows for a total displacement of +129 to -126 from the jump relative OP code address. Another major advantage is that it allows for relocatable code.

Extended Addressing

Extended Addressing provides for two bytes (16 bits) of address to be included in the instruction. This data can be an address to which a program can jump or it can be an address where an operand is located.

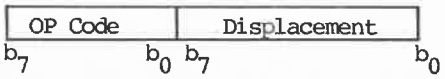


Extended addressing is required for a program to jump from any location in memory to any other location, or load and store data in any memory location.

When extended addressing is used to specify the source or destination address of an operand, the notation (nn) will be used to indicate the content of memory at nn, where nn is the 16-bit address specified in the instrucion. This means that the two bytes of address nn are used as a pointer to a memory location.

Indexed Addressing

In this type of addressing, the byte of data following the OP code contains a displacement which is added to one of the two index registers (the OP code specifies which index register is used) to form a pointer to memory. The contents of the index register are not altered by this operation.



An example of an indexed instruction would be to load the contents of the memory location (Index Register + Displacement) into the accumulator. The displacement is a signed two's complement number. Indexed addressing greatly simplifies programs using tables of data since the index register can point to the start of any table. Two index registers are provided since very often operations require two or more tables. Indexed addressing also allows for relocatable code.

The two index registers in the Z80A are referred to as IX and IY. To indicate indexed addressing the notation:

(IX+d) or (IY+d)

is used. Here d is the displacement specified after the OP code. The parentheses indicate that this value is used as a pointer to external memory.

Register Addressing

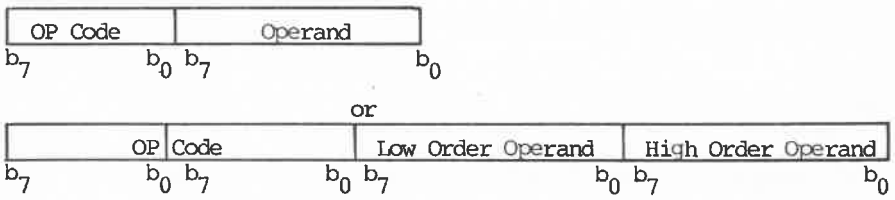
Many of the Z80A OP codes contain bits of information that specify which CPU register is to be used for an operation. An example of register addressing would be to load the data in register B into register C.

Implied Addressing

Implied addressing refers to operations where the OP code automatically implies one or more CPU registers as containing the operands. An example is the set of arithmetic operations where the accumulator is always implied to be the destination of the results.

Register Indirect Addressing

This type of addressing specifies a 16-bit CPU register pair (such as HL) to be used as a pointer to any location in memory. This type of instruction is very powerful and it is used in a wide range of applications.



An example of this type of instruction would be to load the accumulator with the data in the memory location pointed to by the HL register contents. Indexed addressing is actually a form of register indirect addressing except that a displacement is added with indexed addressing. Register indirect addressing allows for simple implementation of powerful memory accesses. The block move and search commands in the Z80A are extensions of this type of addressing where automatic register incrementing, decrementing and comparing has been added. The notation for indicating register indirect addressing is to put parentheses around the name of the register that is to be used as the pointer. For example, the symbol

(HL)

specifies that the contents of the HL register are to be used as a pointer to a memory location. Often register indirect addressing is used to specify 16-bit operands. In this case, the register contents point to the lower order portion of the operand while the register contents are automatically incremented to obtain the upper portion of the operand.

Bit Addressing

The Z80A contains a large number of bit set, reset and test instrucions. These instructions allow any memory location or CPU register to be specified for a bit operation through one of three previous addressing modes (register, register indirect and indexed) while three bits in the OP code specify which of the eight bits is to be manipulated.

5.8.3 Addressing Mode Combinations

Many instructions include more than one operand (such as arithmetic instructions or loads). In these cases, two types of addressing may be employed. For example, load can use immediate addressing to specify the source and register indirect or indexed addressing to specify the destination.

5.8.4 Flags

Each of the two Z80A CPU Flag registers contains six bits of information which are set or reset by various CPU operations. Four of these bits are testable; that is, they are used as conditions for jump, call or return instructions. For example a jump may be desired only if a specific bit in the flag register is set. The four testable flag bits are carry, zero, sign and parity. A summary of flag operaions is shown in Table 5-8.

5.9 SYSTEM PROCESSOR BOARD INTERFACE CONNECTIONS AND SCHEMATIC

Appendix J shows the external edge connector pin assignments and jumper configurations for both the System Processor board and BLC-064 RAM board.

The System Processor board schematic is provided in Appendix D.

TABLE 5-8 SUMMARY OF FLAG OPERATIONS

INSTRUCTION	C	Z	P/V	S	N	H	COMMENTS
ADD A,s; ADC A,s	§	§	V	§	0	§	8-bit add or add with carry
SUB s; SBC A,s, CP s, NEG	§	§	V	§	1	§	8-bit subtract, subtract with carry, compare and negate accumulator
AND s	0	§	P	§	0	1	Logical operations
OR s; XOR s	0	§	P	§	0	0	And sets different flags
INC s	o	§	V	§	0	§	8-bit increment
DEC m	o	§	V	§	1	§	8-bit decrement
ADD DD,ss	§	o	o	o	0	X	16-bit add
ADC HL,ss	§	§	V	§	0	X	16-bit add with carry
SBC HL,ss	§	§	V	§	1	X	16-bit subtract with carry
RLA; RLCA,RRA,RRCA	§	o	o	o	0	0	Rotate accumulator
RL m; RLC m; RR m; RRC m SLA m; SRA m; SRL m	§	§	P	§	0	0	Rotate and shift location m
RLD, RRD	o	§	P	§	0	0	Rotate digit left and right
DAA	§	§	P	§	o	§	Decimal adjust accumulator
CPL	o	o	o	o	1	1	Complement accumulator
SCF	1	o	o	o	0	0	Set carry
CCF	§	o	o	o	0	X	Complement carry
IN r,(C)	o	§	P	§	0	§	Input register indirect
INI; IND; OUTl; OUTD	o	§	X	X	1	X	Block input and output
INIR; INDR; OTIR; OTDR	o	1	X	X	1	X	Z = 0 if B = 0 otherwise Z = 1
LDI, LDD	o	o	§	o	0	0	Block transfer instructions
LDIR, LDDR	o	o	0	o	0	0	P/V = 1 if BC = 0, otherwise P/V = 0
CPI, CPIR, CPD, CPDR	o	§	§	§	1	X	Block search instructions Z = 1 if A = (HL), otherwise Z = 0 P/V = 1 if BC = 0, otherwise P/V = 0
LD A,I; LD A,R	o	§	IFF	§	0	0	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag
BIT b,s	o	§	X	X	0	1	The state of bit b of location s is copied into the Z flag

NOTE: The following notation is used in this table.

SYMBOL	OPERATION
C	Carry/link flag. C=1 if the operation produced a carry from the MSB of the operand or result.
Z	Zero flag. Z=1 if the result of the operation is zero.
S	Sign flag. S=1 if the MSB of the result is one.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V=1 if the result of the operation is even, P/V=0 if result is odd. If P/V holds overflow, P/V=1 if the result of the operation produced an overflow.
H	Half-carry flag. H=1 if the add or subtract operation produced a carry into or borrow from into bit 4 of the accumulator.
N	Add/Subtract flag. N=1 if the previous operation was a subtract. H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed DCD format following addition or subtraction using operands with packed BCD format.
§	The flag is affected according to the result of the operation.
o	The flag is unchanged by the operation.

TABLE 5-8 (Cont.)

0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a undefined.
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX and IY.
R	Refresh counter.
n	8-bit value in range <0, 255>.
nn	16-bit value in range <0, 65535>.
m	Any 8-bit location for all the addressing modes allowed for the particular instruction.

Chapter 6

PROGRAMMING INFORMATION FOR FLEXIBLE DISK CONTROLLER BOARD, BLC-8222

6.1 GENERAL INFORMATION

This chapter describes the programming interface for the BLC-8222 Controller Board. The System Processor initiates the board operation by forming and storing Input/Output Parameter Blocks (IOPB) in the external system memory. It then communicates with the controller board by sending, over the system bus, two command bytes for the IOPB starting address.

The controller board internal processor unit (IPU) interrogates the command and accesses the external memory to transfer the block of control data to the board. The IOPB data is received and stored in the on-board memory. This block of information, among other things, tells the controller board the type of data manipulation that is to be performed by the disk drive. The on-board IPU and floppy Disk Controller logic interact to control the read/write operations at the selected disk drive and provide status to the System Processor when the disk operation is complete.

When using the CP/M operating system or the diagnostic program supplied with the MICROSYSTEM 6600, all required programming of the BLC-8222 board is carried out either in the boot firmware or in the disk-resident programs. This chapter is provided to allows users to generate their own programs, if desired.

CAUTION

> The MICROSYSTEM 6600 Hardware is factory configured to operate with the factory supplied software. Changes to hardware jumper assignments, without corresponding changes in system software, will make the hardware and software incompatible, and may make the system inoperable.

6.2 BOARD CONFIGURATION

The controller board hardware must be configured to conform to the system requirements. The board set up involves the physical positioning of DIP switches and placement of jumper connections which program the on-board logic to select the following operating conditions for the system I/O interface:

- Board Address (Base Address) Selection
- Interrupt Request Line Selection
- Drive Size (Standard/Miniature) Selection
- Drive Type (Single/Double Sided) Selection

Appendix B shows the BLC-8222 jumper placement as supplied with the MICROSYSTEM 6600.

Board Address (Base) Selection

The System Processor uses the most significant five bits (ADR3/ - ADR7/) of the lower address byte to address the physical location of the controller board in the System I/O space. This address is called the Base Address. A different Base Address is assigned for each printed wiring board installed in the System. The Base Address is set by physically positioning the Base Switch, S2, to provide the required hexadecimal value for the system addressing scheme. The incoming address bits ADR 3/-ADR 7/ are compared with the value set in the Base Switch. When these values are equal, the controller board is enabled to respond to the I/O Commands.

Switch position 1 represents the most significant bit (MSB) and position 5 represents the least significant bit (LSB). The Base Address value of 70H is set at the factory. It may be changed by the user to conform to his system programming requirements.

Interrupt Request Line Selection

The controller board sends an interrupt signal to the System Processor whenever it completes the execution of a command or whenever it detects a change in the status of a disk drive. The System Processor can test for the completion of a disk operation by either polling the Busy status bit through the controller board I/O interface, or by enabling the controller board interrupt through the IOPB and then servicing the interrupt when it is sent from the board.

Interrupts to the System Processor are sent over one of eight Interrupt Lines (INTØ/-INT7/). The Interrupt Line is assigned by physically positioning the INT Select switch, S1, to select one of the lines for the board I/O interface. The association between the individual switch positions and interrupt lines is given in Appendix B.

Drive Size (Standard/Miniature) Selection

The controller board must be physically configured to select the disk drive size (8-inch diameter standard, or 5 1/4 - inch diameter miniature) installed in the system. Two jumper connections, W1 and W2, are used to make the selection. However, different size drives cannot be intermixed in the system. Up to four disk drives can be interfaced with the controller board.

Drive Type (Single/Double-Sided) Selection

The controller board must be physically configured to select the disk type, single- or double-sided recording surfaces, for the disk drive installed in the system. A single jumper connection, W3, is used to make the drive selection. Single- and double-sided drives cannot be intermixed in the system.

6.3 INPUT/OUTPUT COMMUNICATIONS

Up to six bytes of information pass over the system bus between the System Processor and Disk Controller board during the addressing phase for I/O operations between these two units. These bytes of information consist of three command bytes and three status bytes.

The I/O addresses range from BASE+0 to BASE+7. The Base value of 70 Hex is established by the setting of Base Switch (S2). This switch interface is used by the System Processor to send three command bytes to the controller board and to read three status bytes sent to the System Processor from the board. The three command bytes are BASE+1, BASE+2 and BASE+7. The three status bytes are BASE+0, BASE+1 and BASE+2. The word format for command and status bytes is described in subsequent paragraphs.

When the System Processor wants the controller board to begin an operation, it sends two command bytes to the controller board. These command bytes contain the address of a location in the external main memory. This location is the starting point of a block of data called the input/output parameter block (IOPB). The first command byte is the lower-order address byte; this byte enters the odd command-in port at address 71H. The second command byte is the higher-order address byte; this byte enters the even command-in port at address 72H.

The controller board reads from and writes to the system external main memory using direct memory access (DMA). The DMA interface is used to transfer IOPB's into the on-board memory and to transfer data blocks between on-board memory and the external main memory. The IOPB may consist of 6 or 12 bytes and contains all the information that is necessary for the controller board to perform the operations required by the System Processor. Commands are received at the Odd/Even Command Ports and Odd/Even Status Ports as shown in Figure 6-1.

The controller board performs the operations specified by the IOPB and generates interrupts to inform the System Processor of the completion of operations and changes in disk status.

6.3.1 Command Word Format

The command provides the controller board with the address of the IOPB that is stored in the system main memory. The word format and addresses for the three input commands, BASE+1, BASE+2 and BASE+7, are presented in Figure 6-2; the bit positions for each command word are included. The function of each command is given in the following paragraphs.

Command Byte BASE+1. An output to this address (71H) specifies the lower address byte pointer to the IOPB in system main memory.

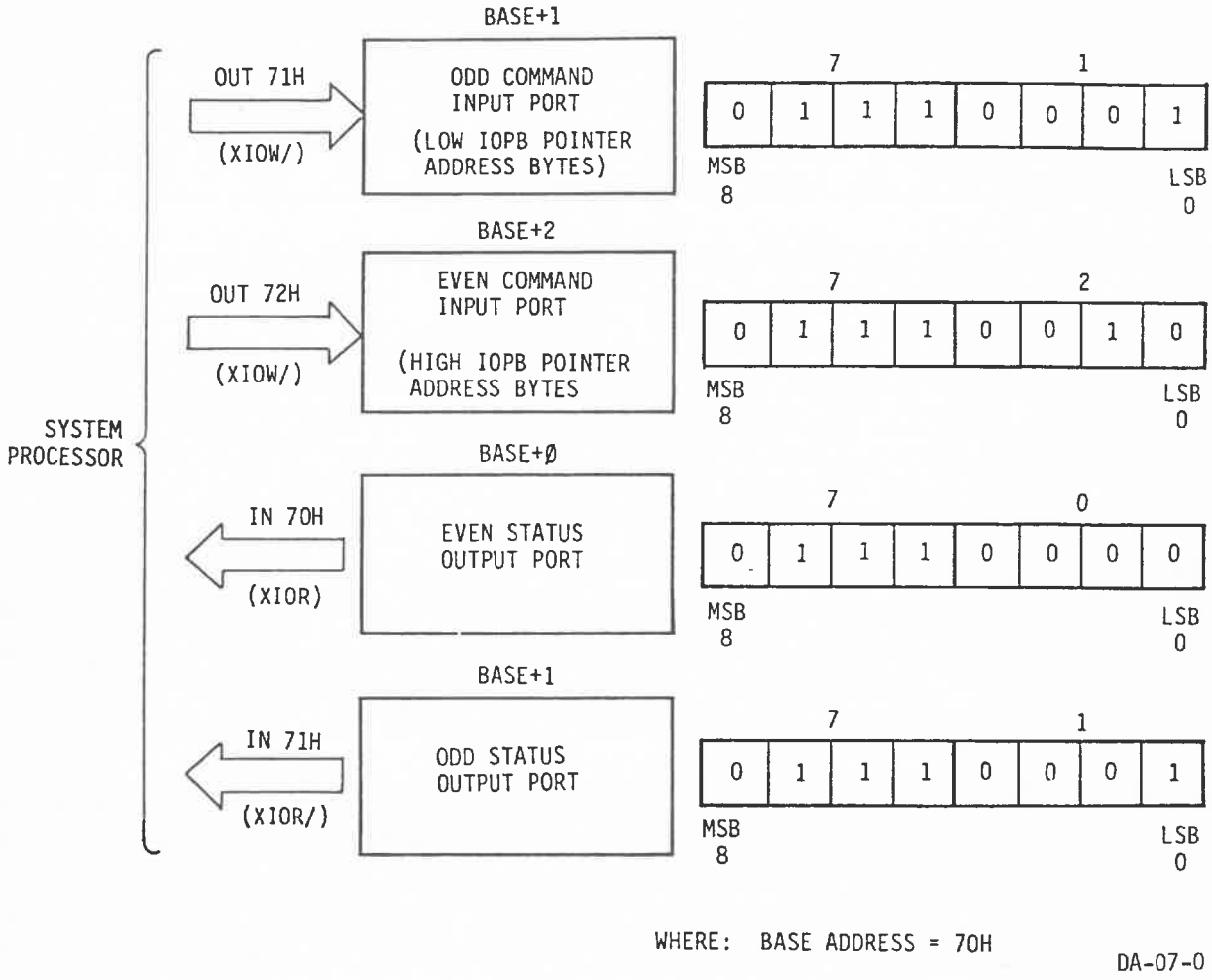


Figure 6-1 Input/Output Ports and Assigned Addresses

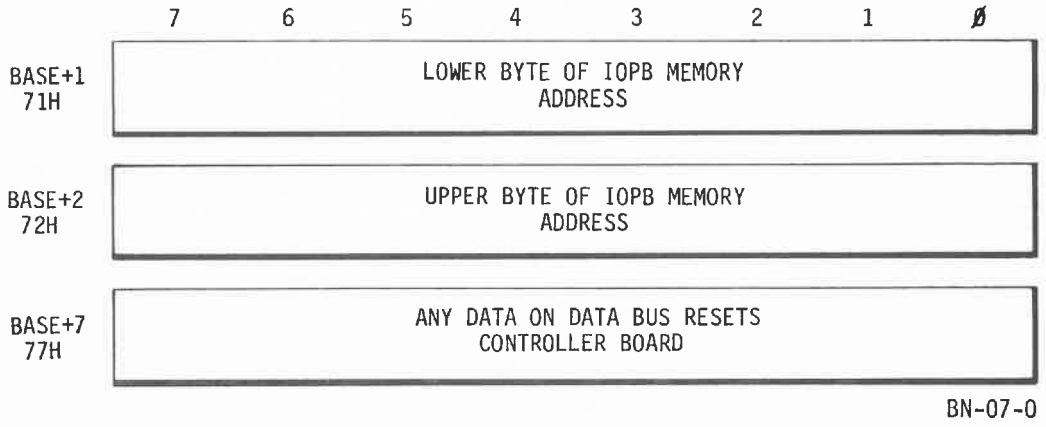

7 6 5 4 3 2 1 Ø
BASE+1 71H
LOWER BYTE OF IOPB MEMORY ADDRESS
BASE+2 72H
UPPER BYTE OF IOPB MEMORY ADDRESS
BASE+7 77H
ANY DATA ON DATA BUS RESETS CONTROLLER BOARD
BN-07-0

Figure 6-2 Word Format for Command Bytes and Associated Addresses

Command Byte BASE+2. An output to this address (72H) performs the same function as the BASE+1 except the byte is the higher address byte of the IOPB pointer; it also interrupts the IPU.

Command Byte BASE+7. An output to this address (77H) causes a system reset of on-board logic independent of the data present on the bus when the command is issued.

6.3.2 Status Word Format

When the controller board completes the operation that is specified by the IOPB, it places status bytes in its status out ports. Word formats and addresses for the three status words, BASE+0, BASE+1 and BASE+2, are presented in Figure 6-3. Note that status words BASE+0 and BASE+2 are also used to provide initialization information for board status.

The status bytes, BASE+0 and BASE+2, are made available by the controller board firmware when the System Processor tries to do an I/O input from these addresses. Since these bytes are provided by the firmware, they should be read when the disk controller is not busy to avoid the possibility of an I/O timeout condition. The following paragraphs define bit positions for status bytes BASE+0 and BASE+2.

Status Byte BASE+0. The hexadecimal value for the upper four bits (7, 6, 5, 4) of the status word are used to represent the Error Group as shown in Table 6-1. Depending upon the Error Group that was detected by the upper four bits, the Error Code for each group is established by the high (1) state for each of the lower four bits (3, 2, 1, 0) of the status word. A definition of the Error Code for lower bit positions is described in Table 6-2.

Status Byte BASE+1. The high (1) and low (0) state for each of the bits (7, 6, 5, 4, 3, 2, 1, 0) in the status word define the busy status for disk drives, error conditions present for commands, and the availability of drive readiness. A definition of each bit state for the byte is described in Table 6-3. The BASE+1 status word is always available through a hardware status latch on the controller board.

Status Byte BASE+2. The upper two bits (7 and 6) in the status word are not used. The lower six bits (5, 4, 3, 2, 1 and 0) specify the Block Tag of the last command that was executed with an error.

6.3.3 Input/Output Parameter Block (IOPB) Format

The start of any disk operation occurs when the System Processor writes out to the controller board through I/O addresses BASE+1 and BASE+2 which define the starting address of the IOPB. The IOPB can be located anywhere in the system main memory and consists of either 6 or 12 consecutive bytes of control information. The System Processor determines its size. The diagram in Figure 6-4 shows the format of a 12-byte IOPB. In the event that a 6-byte IOPB is sent, some of the parameters that are variable in the 12-byte IOPB become fixed, or provide a specific condition in the 6-byte IOPB. The following list contains the parameters that have a fixed or given value for the 6-byte IOPB.

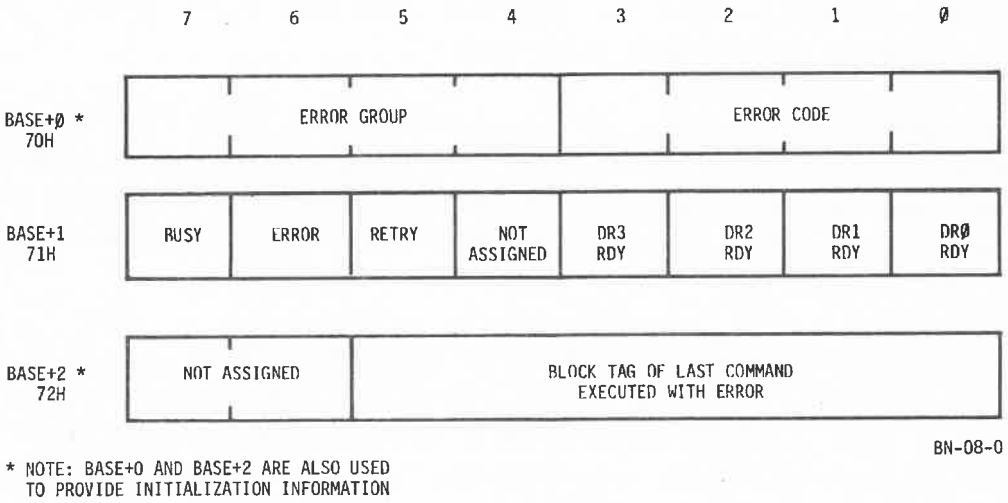


Figure 6-3 Word Format for Status Bytes and Associated Addresses

TABLE 6-1 BASE+0, DEFINITIONS OF ERROR GROUP (BITS 7, 6, 5, 4)

*ERROR GROUP	BIT PATTERN	GLOBAL ERROR CONDITION DETECTED FOR GROUP
F	1111	Change in drive status
C and D	1100 and 1101	IOPB error
B	1011	Seek, restore, or stepping error
A	1010	Read-Write error
9	1001	Write Sector-Format error
*NOTE: Where hexadecimal value indicates the specific group.		

TABLE 6-2 BASE+0, DEFINITIONS OF ERROR CODE (BITS 3, 2, 1, 0)

ERROR GROUP	BIT	*BIT STATE	MEANING
F	3	High (1)	Indicates the status if disk drive 3 has changed.
F	2	High (1)	Indicates the status if disk drive 2 has changed.
F	1	High (1)	Indicates the status if disk drive 1 has changed.
F	0	High (1)	Indicates the status if disk drive 0 has changed.
D	0	High (1)	Indicates an error in sector length.
C	3	High (1)	Indicates an error in the disk command.
C	2	High (1)	Indicates an error in sector number.
C	1	High (1)	Indicates an error in track number
C	0	High (1)	Indicates an error in the number of sectors.
B	2	High (1)	Indicates a seek, step, or restore CRC error; i.e., CRC error present in ID field.
B	1	High (1)	Indicates a seek error.
B	0	High (1)	Indicates selected drive is not ready.
A	3	High (1)	Indicates a loss of data, resulting, perhaps, from an error in hardware timing.
A	2	High (1)	Indicates a read-write CRC error: i.e., an error in the data field.
A	1	High (1)	Indicates that record was not found: i.e., the specific sector to be read from or written into is missing.
9	0	High (1)	Indicates a write-protect error in format or write sector.
*NOTE: Where the Low (0) bit state indicates no error is present.			

TABLE 6-3 BASE+1, DEFINITIONS OF DRIVE/COMMAND STATUS (BITS 7-0)

BIT	BIT STATE	MEANING
7	High (1)	Indicates that the disk controller is busy executing a command.
	Low (0)	Indicates that the last command specified by the IOPB has been executed.
6	High (1)	Indicates that the command executed had an error.
	Low (0)	Indicates the successful execution of a command.
5	High (1)	Indicates that the executed command had a retry.
	Low (0)	Indicates that the command was executed without a retry.
4	---	Unassigned.
3	High (1)	Indicates that drive 3 is ready.
	Low (0)	Indicates that drive 3 is not ready.
2	High (1)	Indicates that drive 2 is ready.
	Low (0)	Indicates that drive 2 is not ready.
1	High (1)	Indicates that drive 1 is ready.
	Low (0)	Indicates that drive 1 is not ready.
0	High (1)	Indicates that drive 0 is ready.
	Low (0)	Indicates that drive 0 is not ready.

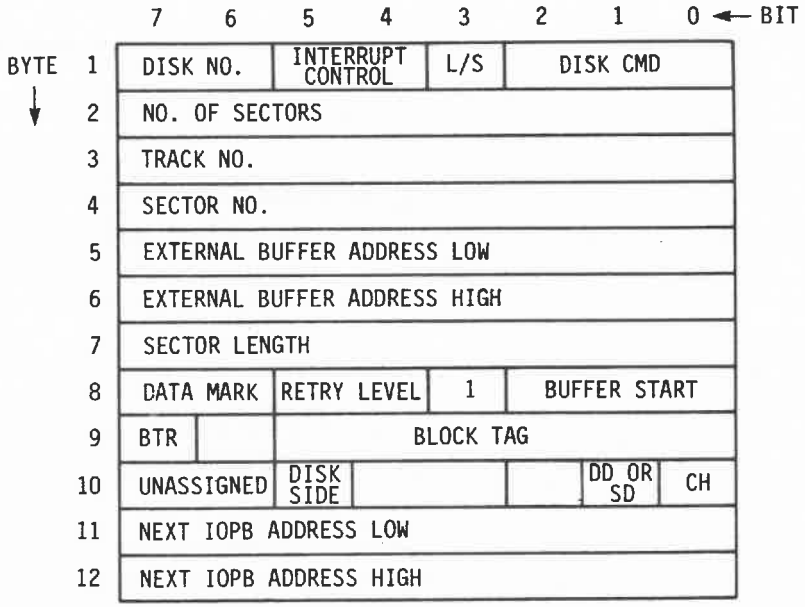

7 6 5 4 3 2 1 0 ← BIT
BYTE
1 DISK NO. INTERRUPT CONTROL L/S DISK CMD
2 NO. OF SECTORS
3 TRACK NO.
4 SECTOR NO.
5 EXTERNAL BUFFER ADDRESS LOW
6 EXTERNAL BUFFER ADDRESS HIGH
7 SECTOR LENGTH
8 DATA MARK RETRY LEVEL 1 BUFFER START
9 BTR BLOCK TAG
10 UNASSIGNED DISK SIDE DD OR SD CH
11 NEXT IOPB ADDRESS LOW
12 NEXT IOPB ADDRESS HIGH
WHERE ABBREVIATIONS ARE AS FOLLOWS:
L/S=LONG (12-BYTE)/SHORT (6-BYTE) IOPB
BTR=BLOCK TAG REPORT BIT
DD=DOUBLE DENSITY
SD=SINGLE DENSITY
CH=CHAINING
IOPB=I/O PARAMETER BLOCK
BN-09-0

Figure 6-4 Input/Output Parameter Block, 12-Byte Format

- Sector length = 256 Bytes
- Data Mark = FBH (Normal Data Mark)
- Retry Level = 3 (x 4 for a total of 12 retries)
- No chaining of IOPB's
- IBM Format only
- Single Density, Single-Sided Diskette only

The relative positioning of bytes within the IOPB and the definitions of bit settings for each byte is presented in Table 6-4.

6.3.4 Interface Operation

The set of six command and status bytes is passed between the System Processor and the controller board through the I/O interface to control the board operations. The System Processor forms an IOPB for a particular desired disk operation. It then sends two command bytes, OUT BASE+1 and OUT BASE+2, to the Odd and Even command input ports respectively.

Where:

BASE+1 = The Odd Command input port of Low IOPB pointer address bytes
BASE+2 = The Even Command input port of High IOPB pointer address bytes

The output to BASE+1 and BASE+2 generates an interrupt for the on-board internal processor (IPU) and sets a bit in the status byte residing at address BASE+1. This bit is called the BUSY bit. The on-board IPU picks up the IOPB pointer address. A twelve-byte DMA is always performed by the board logic to transfer the IOPB from the system memory to the on-board memory. The IOPB is decoded for the command specified. Upon completion of the command, STATUS bytes are placed for the System Processor at addresses BASE+0 and BASE+1. These are to inform the System Processor whether the command has been completed successfully or not. The BUSY bit is reset to inform the System Processor that the command has been executed. An interrupt is generated for the System Processor if specified in the IOPB. The controller board then goes into an idle loop waiting for another command from the System Processor. Meanwhile, the System Processor, after sending in the two COMMAND bytes, can either wait for an interrupt from the controller board to signify the end of the command or poll the BUSY bit until it resets. The following program specifies the System Processor operation; assume the IOPB specifying a READ disk command is residing in the system memory starting location 4000H. The System Processor will execute the following code:

```
XRA     A       ;   REG A = IOPB low address byte
OUT     71H     ;   BASE=70H; 71=BASE+1; Command byte
MVI     A,40H   ;   REG A = IOPB high address byte
OUT     72H     ;   72=BASE+2; Command byte
```

This code provides the controller board with the pointer to the IOPB location in the main memory; after executing this code, the System Processor has two options as follows:

TABLE 6-4 INPUT/OUTPUT PARAMETER BLOCK (IOPB), BYTE AND BIT DEFINITIONS

BYTE	BIT(S)	BIT STATE	DEFINITION
1	7, 6		These two bits define which drive is to be selected.
		00	In this state, these bits select disk drive 0.
		01	In this state, these bits select disk drive 1.
		10	In this state, these bits select disk drive 2.
		11	In this state, these bits select disk drive 3.
	5, 4		These two bits specify when to interrupt the System Processor.
		00	This code tells the controller board never to interrupt the System Processor.
		01	This code means that the controller board may interrupt the System processor only in the event of an error.
		10	This code means that the controller board may interrupt the System Processor only after each IOPB.
		11	This code means that the controller board may interrupt the System Processor either after the last IOPB or in the event of an error.
	3		This bit specifies the length of bytes in IOPB.
		0	This state tells the controller board firmware that the current IOPB is 6 bytes in length.
		1	This state tells the controller board firmware that the current IOPB is 12 bytes in length.
	2, 1, 0		These three bits specify the type of disk command issued by System Processor.
		000	This code indicates that the System Processor wants to transfer data from the selected disk to the main memory.
		001	This code indicates that the System Processor wants a transfer from main memory to the selected disk.
		010	This code tells the controller board to format the selected track sequentially.
		011	This code tells the controller board to format the selected track randomly (i.e., non-sequentially).
		100	This code tells the controller board to transfer data from its on-board buffer to main memory.
		101	This code tells the controller board to transfer data from the main memory to the on-board buffer.

TABLE 6-4 (cont.)

BYTE	BIT(S)	BIT STATE	DEFINITION
1 (cont)	2, 1, 0	110	This code tells the controller board to run a disk read-write test routine.
		111	This code is unassigned.
2	7-0	various	This entire byte contains the code that indicates the number of sectors to be written on or read from a diskette. Number of sectors must be one or greater; 0 is illegal.
3	7-0	various	This byte indicates the starting number of the track on the diskette currently involved in data transfer. For a miniature disk drive, the track numbers range from 0 to 34. For a standard disk drive, the numbers range from 0 to 76.
4	7-0	various	This byte indicates the starting number of a particular sector. The range depends on the lengths of the sectors and must be 1 or any legal number.
5	7-0	various	This byte is the lower address of the location in the external memory that is used as a buffer during data transfers.
6	7-0	various	This byte is the higher address of the buffer in the external memory. Bytes 5 and 6 form a pointer that points to the location: 1) from where data is obtained for transfer to a diskette 2) where data from a diskette is stored 3) where random sector numbers for random format are obtained 4) where data is obtained for a transfer from the buffer to the on-board buffer. 5) where data is stored during a transfer from the on-board buffer to the main memory.
7	7-0	various	This byte specifies the length of sectors for IBM formats, as indicated: IBM format: 01H = 128 bytes 02H = 256 bytes 03H = 512 bytes Only these codes are allowed for IBM format.
8	7, 6		These two bits specify which data mark is written into the data field of a given sector.
		00	This code specifies a data mark of F8H which indicates a deleted data mark.
		11	This code specifies a data mark of FBH which indicates that the data field is normal.

TABLE 6-4 (cont.)

BYTE	BIT(S)	BIT STATE	DEFINITION
8 (cont)	5, 4		These two bits specify the retry level which is the number of times the controller board is to try to complete a command in case of an error.
		00	This code indicates no retry after the first attempt.
		01	This code indicates four retries.
		10	This code indicates eight retries.
		11	This code indicates 12 retries.
	3		This bit specifies an IBM format.
		1	This state indicates an IBM format.
		0	This state is illegal.
	2, 1, 0		These three bits specify the number of bytes to be transferred between external memory and the on-board buffer memory. This data is transferred in blocks of 128 bytes as determined by the type of command specified by Byte 1 for commands 4 and 5 (code 100 and 101).
		000	This code indicates a transfer of 8 blocks starting from block 0.
		001	This code indicates a transfer of 7 blocks starting from block 1.
		010	This code indicates a transfer of 6 blocks starting from block 2.
		011	This code indicates a transfer of 5 blocks starting from block 3.
		100	This code indicates a transfer of 4 blocks starting from block 4.
		101	This code indicates a transfer of 3 blocks starting from block 5.
		110	This code indicates a transfer of 2 blocks starting from block 6.
		111	This code indicates a transfer of 1 block starting from block 7.
	7		This bit specifies whether or not the block tag of a block is to be reported in the event of an error.
		0	This state indicates that the block tag is not to be reported.
		1	This state indicates that the block tag is to be reported.
	6	--	This bit is unassigned.
	5-0	various	Knowing the block tag of a block of bytes allows the System Processor to associate an I/O complete interrupt request from the controller board with a specific block of data when chained IOPB's are used. This is necessary in the event of an error.

TABLE 6-4 (cont.)

BYTE	BIT(S)	BIT STATE	DEFINITION
10	7, 6	--	These two bits are unassigned.
	5		This bit specifies the side to use when a double-sided diskette is used.
		0	This state indicates the selection of side 0.
		1	This state indicates the selection of side 1.
	4,3,2	--	These three bits are unassigned.
	1		This bit specifies single or double density format.
		1	This state indicates double density.
		0	This state indicates single density.
	0		This bit specifies the chaining of IOPB's.
		0	This state indicates that the current IOPB is the last IOPB.
		1	This state indicates that more IOPB's will follow the current IOPB.
11	7-0	various	This byte specifies the 8 least significant bits of the 16-bit main memory address pointing to the beginning of the next IOPB in the chain.
12	7-0	various	This byte specifies the 8 most significant bits of the 16-bit main memory address pointing to the beginning of the next IOPB in the chain.

a. To go into a HALT state and wait for an interrupt from the controller board.

b. To run a polling loop to test the BUSY bit for a reset condition at the controller board STATUS port address, BASE+1.

If either of the above conditions are met, the System Processor checks whether the command has been executed successfully or not. The System Processor executes the following code to check for reset of the BUSY bit and for completion of a successful execution:

Polling to check reset of BUSY bit:

```
BACK:   IN    71H       ;     Load REG A from BASE+1, status byte
        ANI   80H       ;     Establish the BUSY bit
        JNZ   BACK      ;     If BUSY bit = 1, poll again
        JMP   CMDCHK    ;     Else jump to routine which checks if the execution
                              is successful
```

Checking for successful execution:

```
CMDCHK: IN    70H       ;     Load REG A from BASE+0, status byte
        ANA   A         ;     Check if REG A is Zero
        JNZ   ERROR     ;     If not, zero execution is with an error
```

If the system is using chained IOPB, an input of STATUS from BASE+2 provides the BLOCK TAG specifying the link in the chain where the error occurred.

The controller board can be RESET with any output on the address BASE+7; i.e., the execution of an instruction 'OUT 77H' (where BASE = 70H) causes the controller board to be RESET. After a reset, all on-going processes cease and the controller board executes its initialization routine.

Data transfer during Read/Write disk operations is done via DMA. The System Processor needs only to 'START' and check progress of a command, or if using the interrupts, service the interrupt generated by the controller board at the end of the operation.

Figure 6-5 presents a flow chart explaining the processes involved in the System Processor from the moment a command is issued to the controller board until the command is executed. The events that take place in the flow chart are seen from the point of view of the System Processor. For example, in Step 1, the System Processor forms the IOPB in the RAM memory, and, in Steps 2 and 3, the System Processor outputs the address of the IOPB to the controller board. The controller board receives the command and responds to the System Processor by posting its status in Steps 4, 5 and 6. The System Processor interrogates the status for successful completion of the command in Steps 7 and 8, or for an incomplete condition, in which case, the System Processor identifies the type of error present in Step 9.

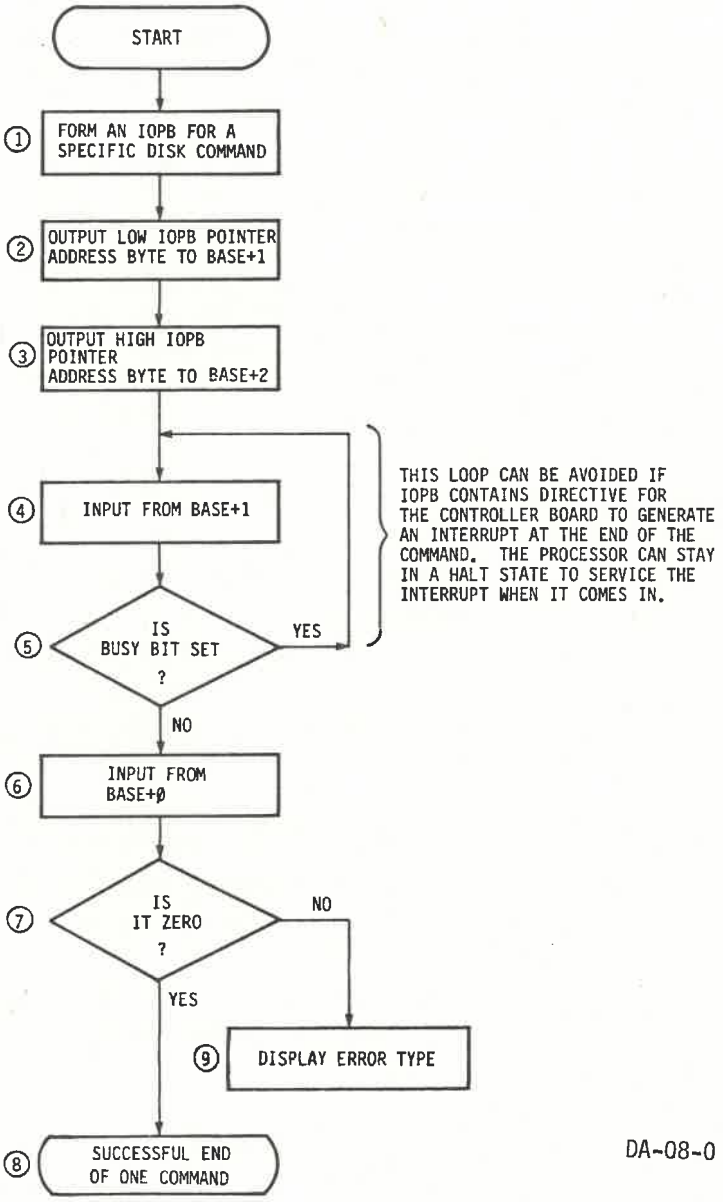

START
1
FORM AN IOPB FOR A SPECIFIC DISK COMMAND
2
OUTPUT LOW IOPB POINTER ADDRESS BYTE TO BASE+1
3
OUTPUT HIGH IOPB POINTER ADDRESS BYTE TO BASE+2
4
INPUT FROM BASE+1
5
IS BUSY BIT SET ?
YES
NO
6
INPUT FROM BASE+Ø
7
IS IT ZERO ?
NO
YES
9
DISPLAY ERROR TYPE
8
SUCCESSFUL END OF ONE COMMAND
THIS LOOP CAN BE AVOIDED IF IOPB CONTAINS DIRECTIVE FOR THE CONTROLLER BOARD TO GENERATE AN INTERRUPT AT THE END OF THE COMMAND. THE PROCESSOR CAN STAY IN A HALT STATE TO SERVICE THE INTERRUPT WHEN IT COMES IN.
DA-08-0

Figure 6-5 Flow Chart for System Processor Interface to Controller Board

6.4 FIRMWARE PROGRAM OPERATION

The flow chart for the Disk Controller overall firmware operations is presented in Figure 6-6. The following steps describe the sequence of events that occur to initialize and select disk drives for operation.

1. During power-up sequence test the RAM and PROM, detect the type of drives installed, prepare drive status, and insert a 2-second time delay for the disk drive motor to come up to speed.

2. If miniature drives are installed, turn off motor, scan the drive status and check for System Processor interrupt.

3. If System Processor interrupts to send IOPB, get IOPB and check parameters' limit.

4. If IOPB is valid, decode the command and complete the task.

5. After completion of the command, send the status to System Processor and interrupt System Processor if required.

6. Keep the drive selected for 1 second to process another IOPB.

7. At this time, if there is another IOPB, process it, otherwise deselect the drive and find "CHANGE DISK" status for standard floppy drives only. Prepare the status and send to System Processor if required.

8. If miniature drives are present, the firmware does not detect "CHANGE DISK" status, but keeps the miniature drive motor on for approximately 3 minutes to process the next IOPB. During the 3-minute interval, update the drives' status. If there is no IOPB during the 3-minute period, turn the miniature drive motor off.

9. Jump to the Idle loop.

A detailed description is provided in subsequent paragraphs for the following firmware operations:

- Initialization Routine
- Idle Loop Routine
- Command Decoding Routine

6.4.1 Initialization Routine

The controller board can be reset by either a POWER-ON, SYSTEM Reset, or a RESET command. Upon being reset, the board executes the Initialization Routine (Figure 6-7) which performs the following operations sequentially:

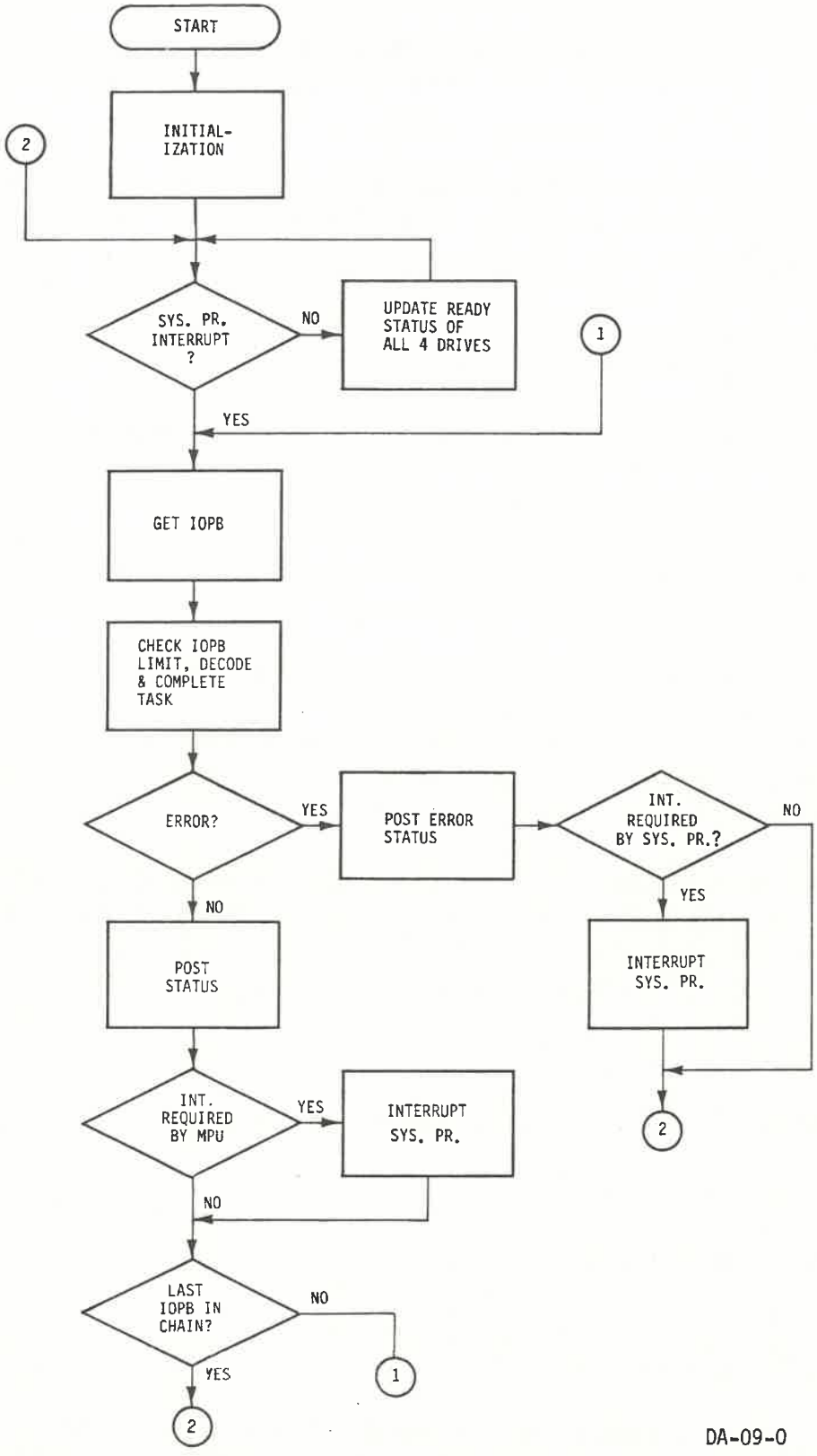


Figure 6-6 Flow Chart for Firmware Operations

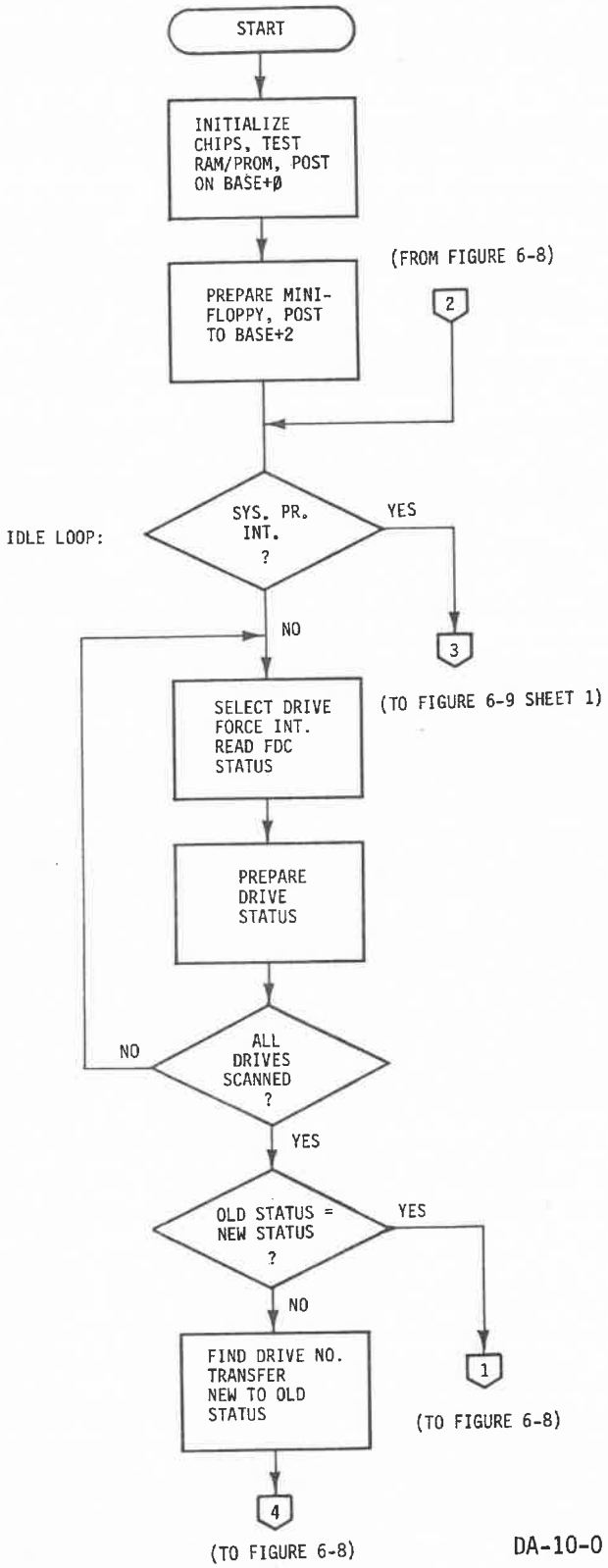


Figure 6-7 Initialization and Idle Loop Flow Chart

1. It initializes all on-board chips, such as resetting flip-flops, clearing registers, etc.

2. It sets the BUSY bit at I/O Port BASE+1. This action prevents any intervention by external sources.

3. It performs a checksum test of on-board ROM to verify that no digits have been changed since the last summation.

4. It performs a memory test of on-board RAM to verify that data can be written into or read from each memory cell.

5. It checks status of the Floppy Disk Formatter/Controller chip to verify its availability to process commands.

6. It places the initialization status byte at port BASE+0 which indicates the following information:

7	6	5	4	3	2	1	Ø (LSB)
1	Ø	X	Ø	X	Ø	X	Ø

BIT 7, WHEN 1, MEANS STATUS HAS BEEN POSTED
BIT 6, IS ALWAYS Ø
BIT 5, WHEN 1, MEANS FD1791 PASSED ITS TEST; Ø MEANS FAILURE
BIT 4 IS ALWAYS Ø
BIT 3, WHEN 1, MEANS ON-BOARD RAM's PASSED TESTS; Ø MEANS FAILURE
BIT 2 IS ALWAYS Ø
BIT 1, WHEN 1, MEANS THAT ON-BOARD ROM PASSED ITS TEST; Ø MEANS FAILURE
BIT Ø IS ALWAYS Ø

If the byte in status port BASE+Ø has a hex value of AA (1010 1010) it indicates that all tested elements on the controller board passed their tests. As shown in the flow chart in Figure 6-7, following initialization, the controller board starts running in its idle loop; during this activity, the controller board constantly checks the ready status of each drive. If the controller board detects a change in status, it prepares to report this change to the System Processor but the controller board doesn't actually report the status of the drives to the System Processor until after the controller board has executed one command. The controller board waits this long to insure that the System Processor has picked up the status byte that the controller board outputted during initialization.

7. It reads the disk configuration as set by on-board switches and jumpers.

8. It prepares BASE+2 Status byte and stores it in the on-board memory. This byte will be posted when requested by System Processor and contains the following information:

7	6	5	4	3	2	1	Ø (LSB)
Ø	Ø	Ø	Ø	X	X	Ø	1

BITS 7, 6, 5 and 4 ARE ALWAYS Ø
BIT 3, WHEN Ø = DUAL HEAD DRIVE TYPE,
1 = SINGLE HEAD DRIVE TYPE
BIT 2, WHEN Ø = STANDARD DRIVE SELECTED,
1 = MINIATURE DRIVE SELECTED
BIT 1 IS ALWAYS Ø
BIT Ø IS ALWAYS 1 TO INDICATE BLC-8222 IS SELECTED

9. It reads disk drive status by polling drives.

10. It inserts a delay of 2.0 seconds to allow drive speed to stabilize for data transfer.

11. It resets the BUSY bit to signal the System Processor that the controller board is ready to accept commands.

Following initialization, the controller board starts running in its Idle Loop. The Idle Loop operation performs a constant check of the ready status of the disk drives. If a change in status is seen, it is immediately communicated to the System Processor via BASE+Ø and BASE+1 and the System Processor is interrupted. The drive ready status, however, is not reported to the System Processor until one IOPB command has been executed. This is to insure that the System Processor has picked up the initial test result byte from I/O Port BASE+Ø before it is changed.

6.4.2 Idle Loop Routine

The controller board operates in an Idle Loop to select the drives and check for ready status. This status is compared with the previous status. If there is any change in status, the controller board interrupts the System Processor, provided at least one command since reset has been executed, otherwise it will not interrupt the System Processor. The Idle loop is repetitively executed until the System Processor interrupts the controller board with the next IOPB address. During the Idle loop, the status of four drives is updated and made available for the System Processor. A flow chart of the Idle Loop operations is presented in Figure 6-8.

6.4.3 Command Decoding Routine

The command decoding routine is shown in the flow chart of Figure 6-9. When the System Processor interrupts the on-board processor, it means there are two command bytes present which direct the pointer to the IOPB location in system memory. By using a DMA operation, the controller firmware

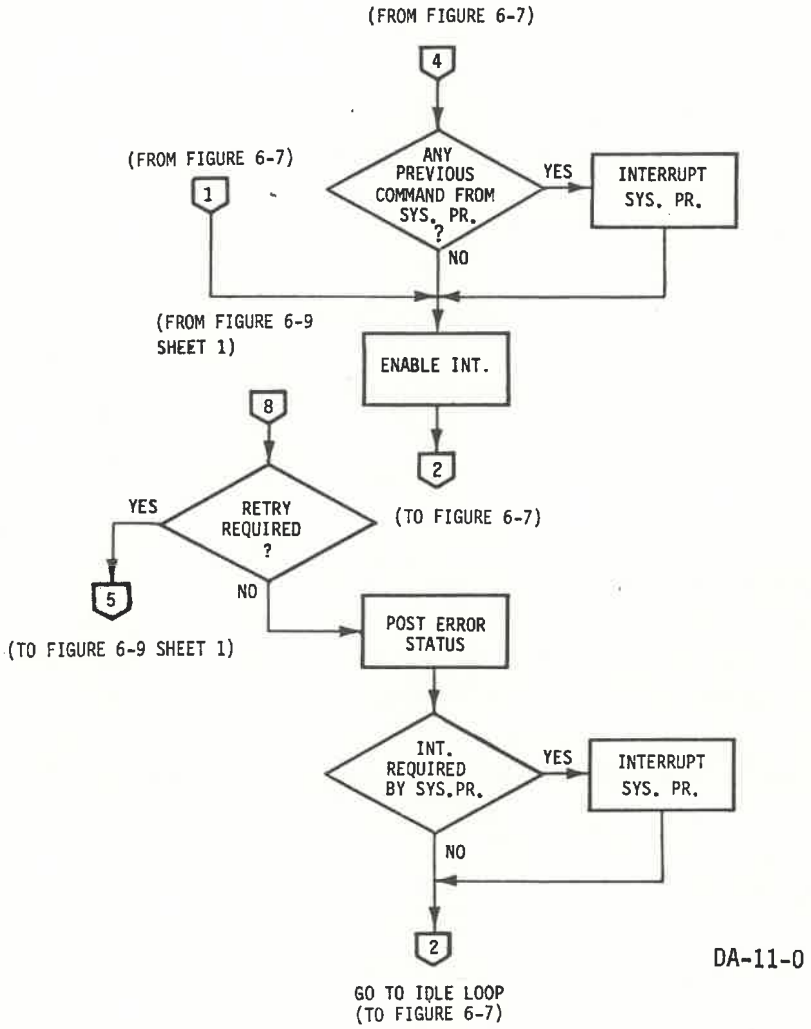


Figure 6-8 Idle Loop Flow Chart

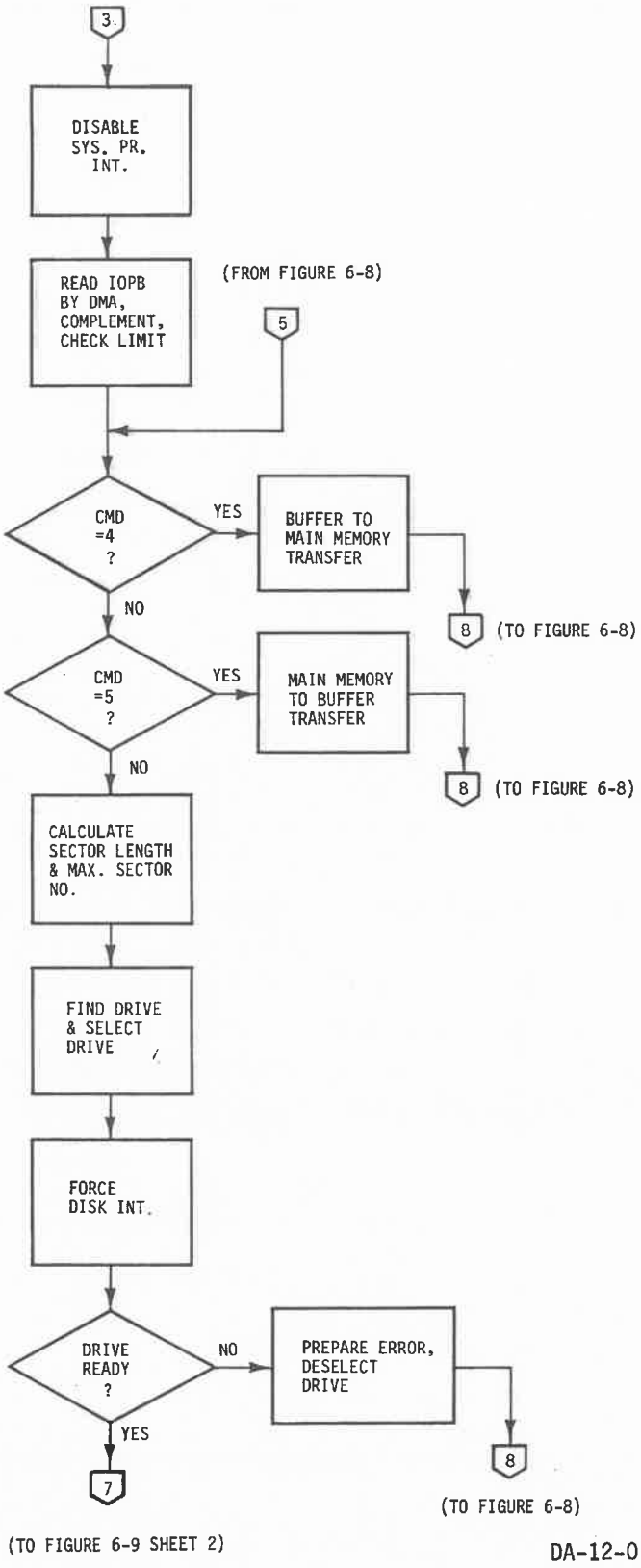


Figure 6-9 Command Decoding Flow Chart (Sheet 1 Of 2)

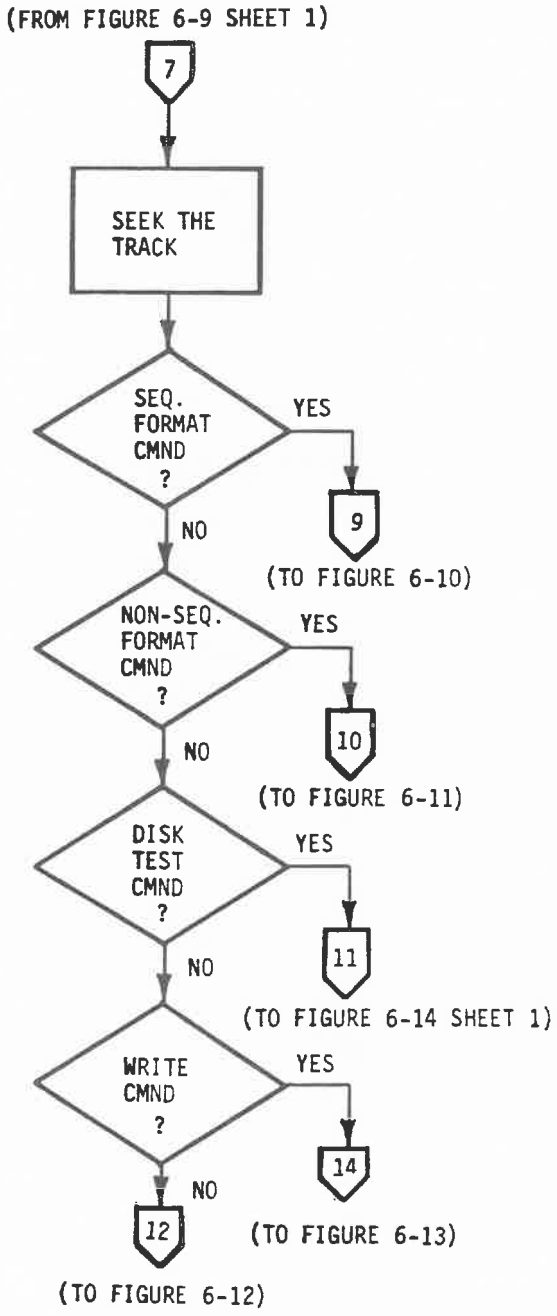


Figure 6-9 Command Decoding Flow Chart (Sheet 2 Of 2)

moves the 12 bytes of IOPB from system memory to the on-board RAM. These IOPB bytes are complimented. The firmware checks for presence of a six or twelve-byte IOPB. In case of a six-byte IOPB, the program assumes the other bytes are defined as follows:

Byte 7, Sector length = 256 bytes

Byte 8, Data mark = FBH (normal data mark)
Retry level = 3
IBM format

Byte 10, Single side, single density

The program checks the limits of the IOPB parameters. If parameters are valid, the program will continue further; otherwise, it will prepare the error status bytes and interrupt the System Processor. The controller board returns to the Idle loop if directed by the System Processor.

6.5 DISK RELATED COMMANDS

When a valid IOPB is present, the disk related commands are separated; and the bytes-per-sector and maximum sectors-per-track are calculated before the command is executed. The disk drive is then selected and the appropriate disk related command is executed. The following commands are described in subsequent paragraphs.

- Disk Format Command
- Disk Read Command
- Disk Write Command
- Disk Test Command

6.5.1 Disk Format Command

The BLC-8222 firmware supports two format types as follows:

1. FM (Single Density) IBM System 3740 Format

2. MFM (Double Density) IBM System 34 Format

The program formats a track by writing the complete track. The sector length can be 128, 256 or 512 bytes. The sector length should be the same for all of the sectors within a diskette. The maximum sector capacity for standard and miniature diskettes is given in Tables 6-5 and 6-6 respectively.

The program also determines the use of a sequential or non-sequential (random) formatting scheme for addressing sectors. If non-sequential formatting is detected, the firmware gets a Random Sector

TABLE 6-5 STANDARD DRIVE SECTOR CAPACITY

SECTOR LENGTH (BYTES)	MAXIMUM SECTORS/TRACK (SINGLE DENSITY)	MAXIMUM SECTORS/TRACK (DOUBLE DENSITY)
128	26	40
256	15	26
512	8	15

TABLE 6-6 MINIATURE DRIVE SECTOR CAPACITY

SECTOR LENGTH (BYTES)	MAXIMUM SECTORS/TRACK (SINGLE DENSITY)	MAXIMUM SECTORS/TRACK (DOUBLE DENSITY)
128	16	20
256	9	16
512	5	9

Table from the external main memory. Then it prepares a table for the FM (single density) or MFM (double density) requirement as shown in Tables 6-7 and 6-8 respectively.

It is recommended that sequential formatting be used for obtaining a faster throughput. For proper skew in sequential and non-sequential formats, refer to the Example Skew Table which follows:

EXAMPLE SKEW TABLE FOR SEQUENTIAL AND NON-SEQUENTIAL FORMATS

TYPE OF DRIVE	SECTOR LENGTH	SKEW IN SINGLE DENSITY	SKEW IN DOUBLE DENSITY
Standard (single head)	128	5	7
	256	3	5
	512	2	3
Standard (dual head)	128	3	5
	256	2	3
	512	1	2
Mini (single & dual head)	128	7	9
	256	4	7
	512	3	4

The use of the Skew Table described in the following example which can be related to the flow charts of Figures 6-10 and 6-11.

EXAMPLE:

Assume that the following conditions are present:

(1) Standard drive (single head)
(2) 256 bytes/sector, double density

From the SKEW TABLE, the number of sectors to be skewed is 5 and would indicate the following requirements for Non-Sequential and Sequential formats:

NON-SEQUENTIAL FORMAT:

1st TRACK

1 2 3 4 5 6 7 8 9 10 11 12 13
14 15 16 17 18 19 20 21 22 23 24 25 26

2nd TRACK

12 13 1 2 3 4 5 6 7 8 9 10 11
24 25 26 14 15 16 17 18 19 20 21 22 23

TABLE 6-7 SECTOR FORMAT FOR FM (IBM SYSTEM 3740) SINGLE DENSITY

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF
6	00
1	FC (Index Mark)
26	FF
*** →	
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number
1	Sector Number
1	Sector Length
1	F7 (2 CRC's written)
11	FF
6	00
1	FB (Data Address Mark)
*No. of Data Bytes	E5 (Data)
1	F7 (2 CRC's written)
27 →	FF
247**	FF

*Number of data bytes = 128, 256 or 512

**Continue writing until FD1791 interrupts out

***Write bracketed field for number of sectors/track

TABLE 6-8 SECTOR FORMAT FOR MFM (IBM SYSTEM 34) DOUBLE DENSITY

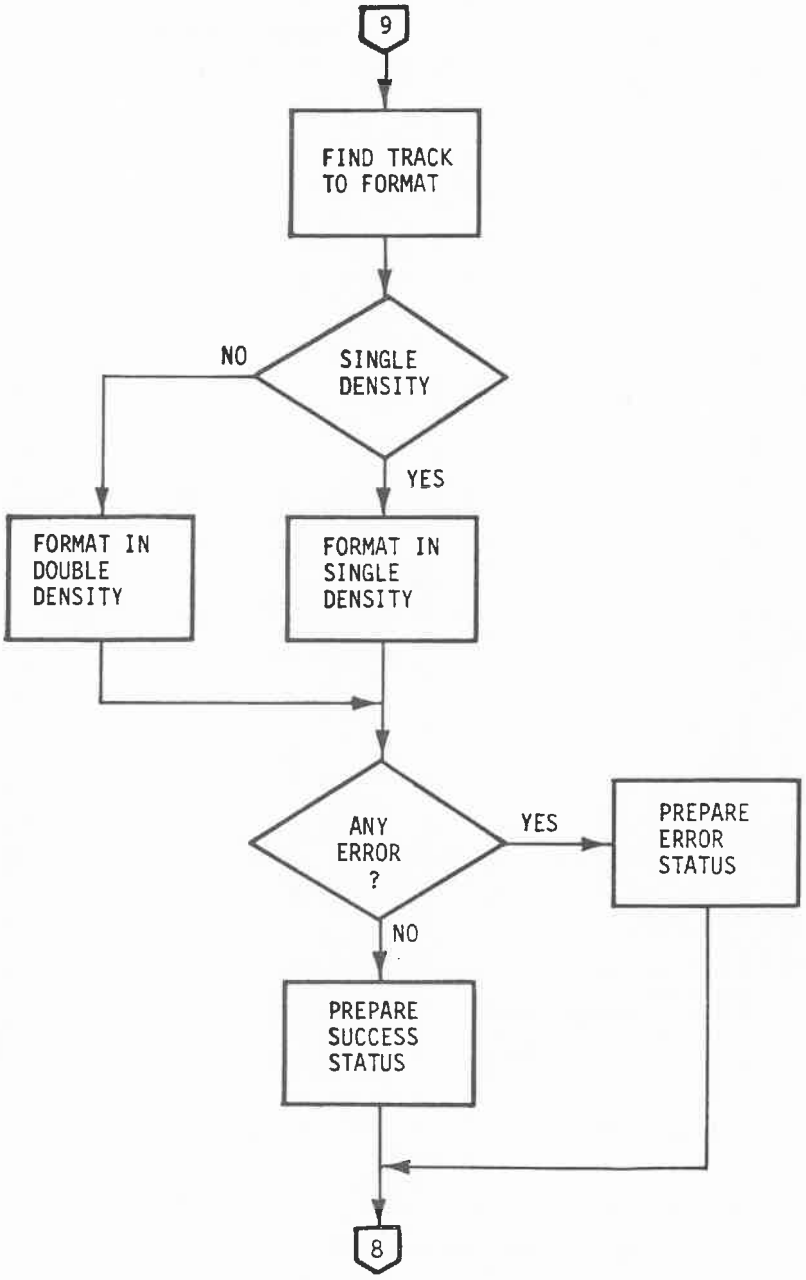
NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50	4E
***	
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number
1	Side Number
1	Sector Number
1	Sector Length
1	F7 (2 CRC's written)
22	4E
12	00
3	F5
1	FB
*No. of Data Bytes	40 (Data)
1	F7 (2 CRC's written)
54	4E
598**	

*Number of data bytes = 128, 256 or 512

**Continue writing until FD1791 interrupts out

***Write bracketed field for number of sectors/track

(FROM FIGURE 6-9 SHEET 2)

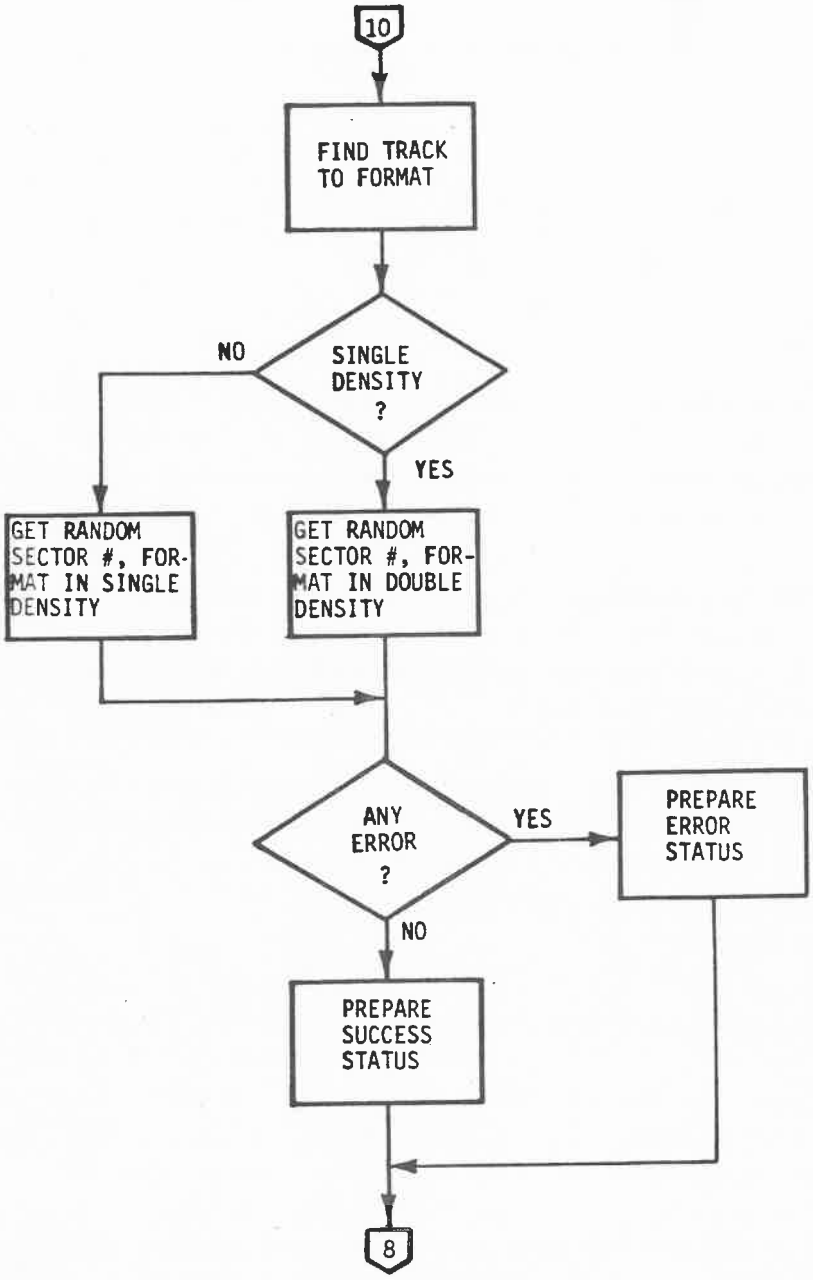


(TO FIGURE 6-8)

CL-25-0

Figure 6-10 Sequential Format Flow Chart

(FROM FIGURE 6-9 SHEET 2)



(TO FIGURE 6-8)

CL-26-0

Figure 6-11 Non-Sequential Format Flow Chart

SEQUENTIAL FORMAT:

1st TRACK

1 2 3 4 5 6 7 8 9 ----------

2nd TRACK

22 23 24 25 26 1 2 3 4 ----------

6.5.2 Disk Read Command

Double buffering via DMA-1 and DMA-2 is used in the Disk Read Command for maximum throughput. Disk transfer to RAM via DMA is set up such that the terminal count is equal to the sector length. The program looks for an interrupt from the disk. After reading one sector, the disk status is examined for any error in the operation. Then the DMA is set up to transfer data from on-board RAM to external main memory via DMA-2. While this operation is being done, the next sector is read in the second buffer area. The first buffer is transmitted to the external memory via DMA-2 while the next sector is being read from the disk into the second buffer by DMA-1. If there is an interrupt from the FD1791 floppy disk controller chip, the program checks the sector number and increases the track number (if required) to read more sectors.

Since the double buffering method is used, a maximum transfer can be achieved in reading a sequentially formatted disk. The Disk Read Command Routine is shown in the flow chart of Figure 6-12.

6.5.3 Disk Write Command

The Disk Write Command is similar to the Disk Read Command. In the Write Command, the controller board gets a sector of data from the external main memory to the RAM buffer via DMA-2. While the data is being written to the disk via DMA-1, the DMA-2 operation continues to get the next sector of data from the external memory. This write operation continues via DMA-2 and DMA-1 until the command is completed or interrupted by the FD1791 floppy disk controller chip.

Since the double buffering method is used, the maximum transfer of data is achieved in writing a sequentially formatted disk. The Disk Write Command Routine is shown in the flow chart of Figure 6-13.

6.5.4 Disk Test Command

The Disk Test Command formats the disk and performs a read/write comparison test for all sector-track locations. A flow chart of the command functions is given in Figure 6-14. These Test Command functions are summarized as follows:

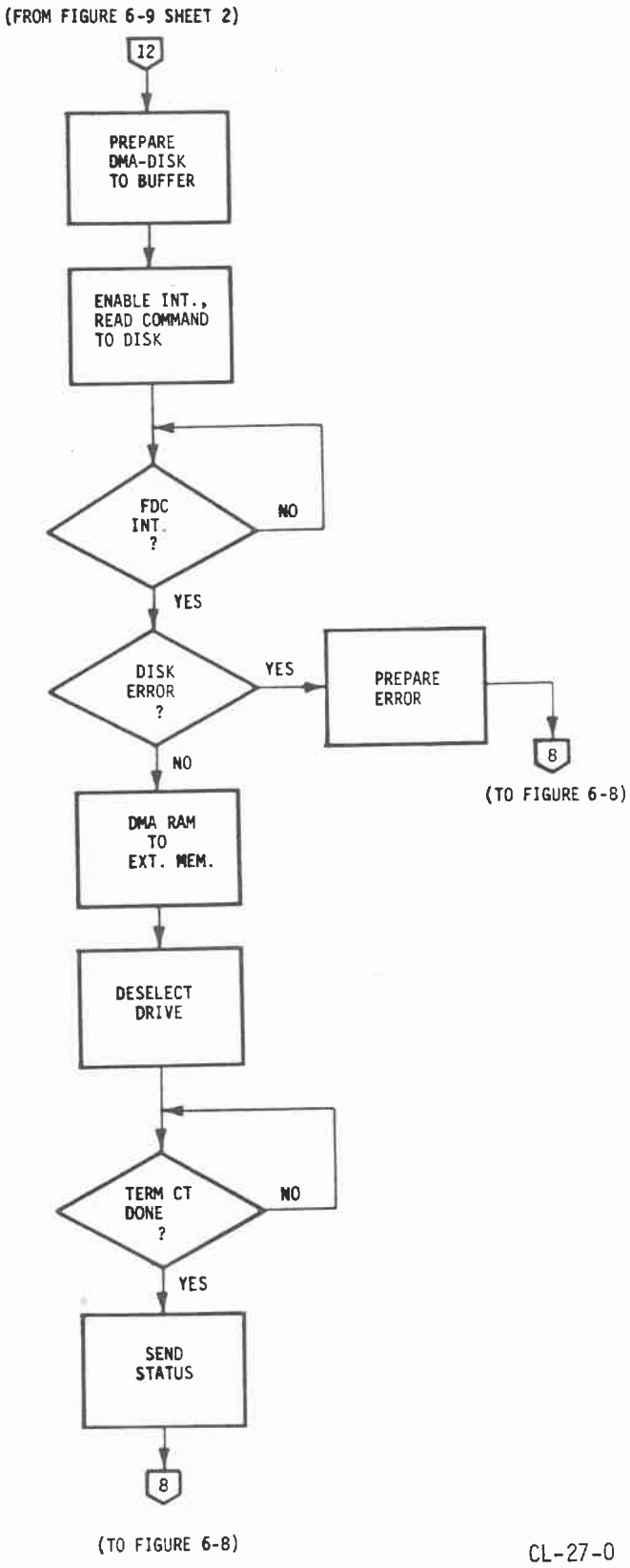
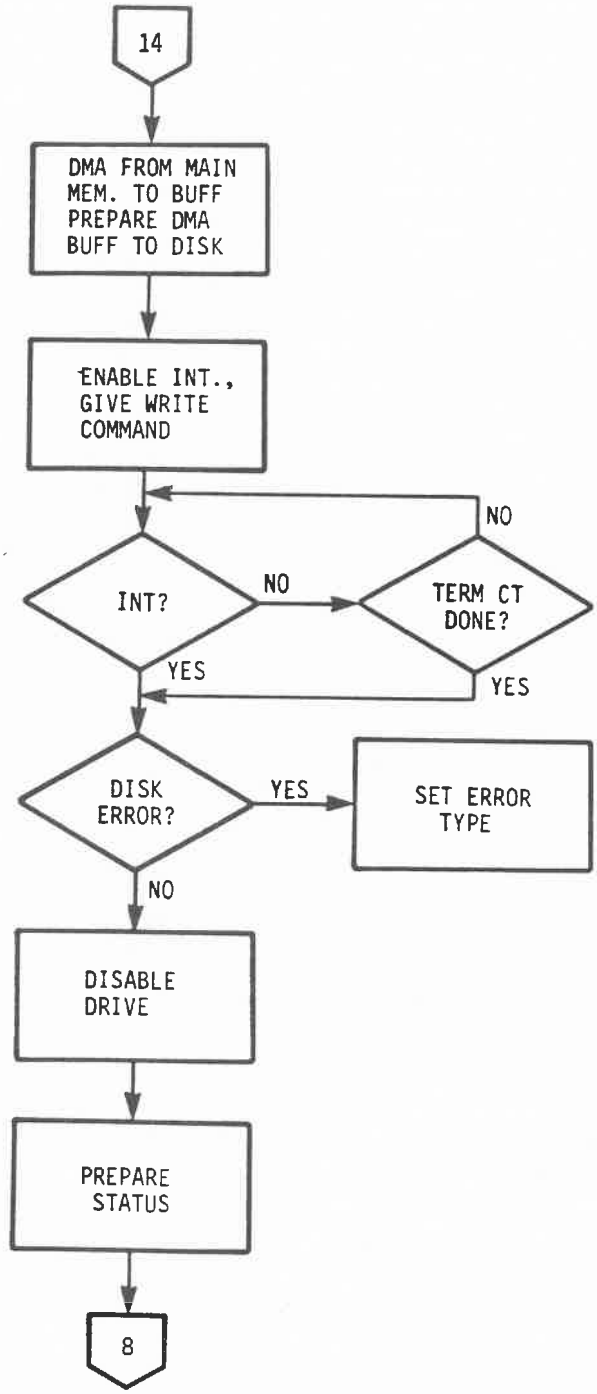


Figure 6-12 Read Command Flow Chart

(FROM FIGURE 6-9 SHEET 2)



(TO FIGURE 6-8)

CL-28-0

Figure 6-13 Write Command Flow Chart

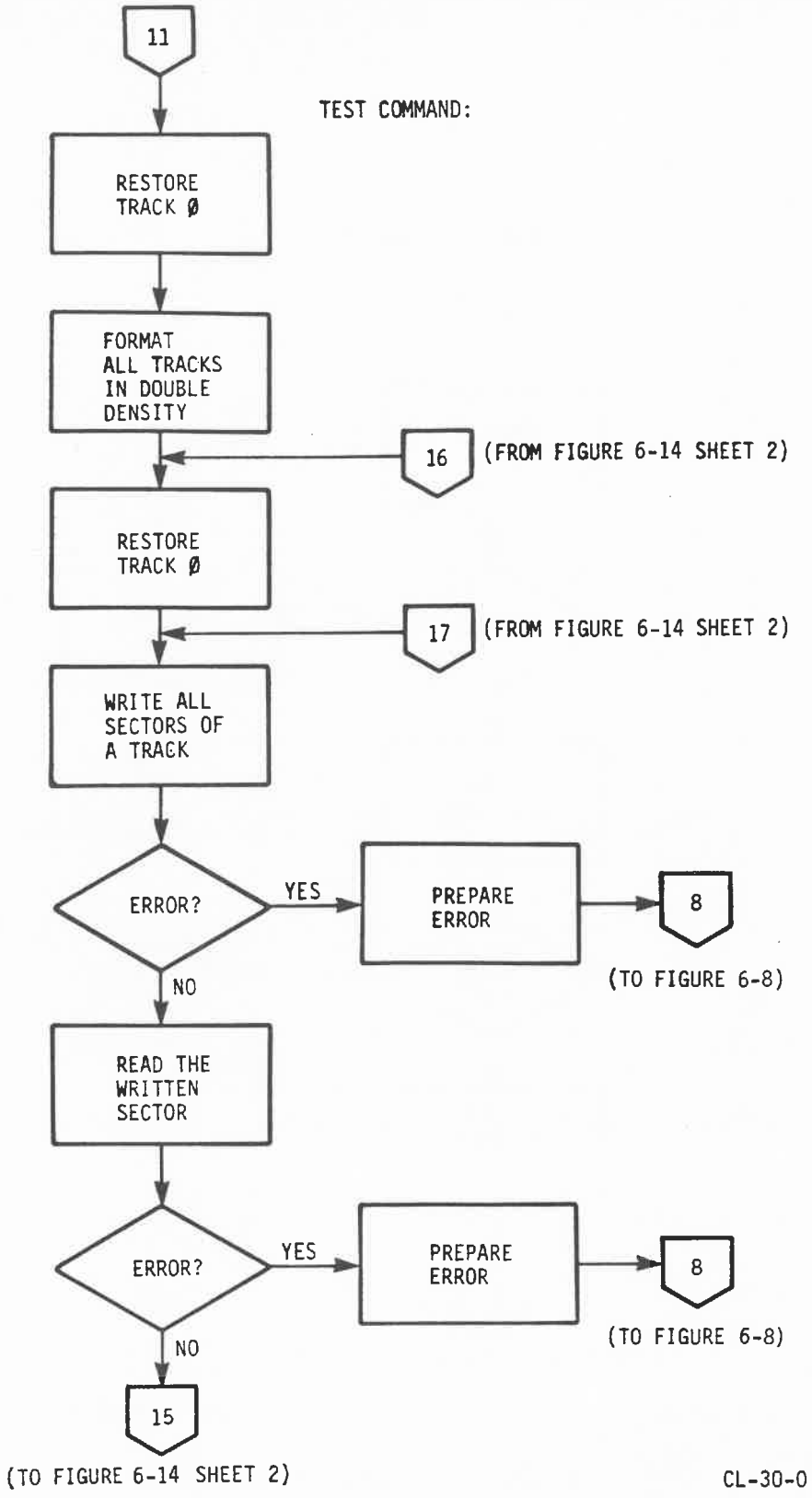
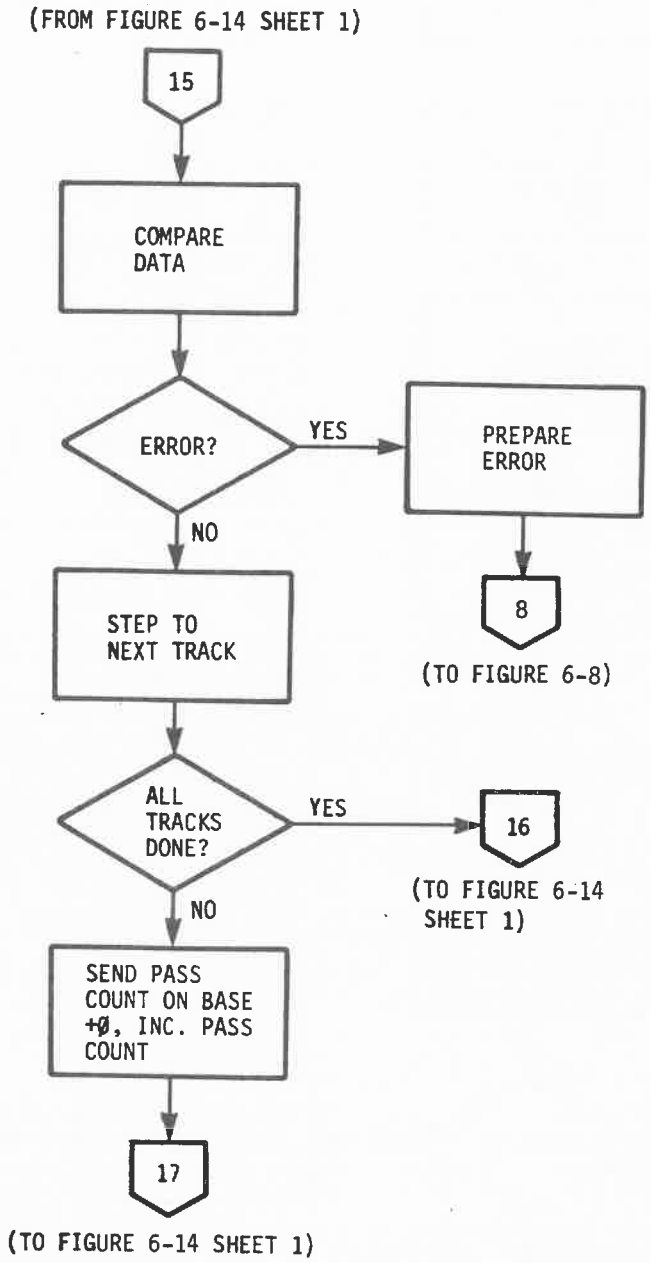


Figure 6-14 Test Command Flow Chart (Sheet 1 Of 2)



CL-29-0

Figure 6-14 Test Command Flow Chart (Sheet 2 Of 2)

1. Select the drive specified in IOPB.

2. Format the disk in double density with 256 bytes/sector

3. Perform write/read and compare test on the disk for every sector of all the tracks. During this operation, if an error occurs, the controller interrupts the System Processor and sends an error status byte. At the end of every pass, the number of passes is posted at BASE+0. For types of errors, refer to Tables 6-3 and 6-4 for BASE+0 Error Codes.

In the test mode, data that is written on the disk within a sector is in an increment of one. The starting data byte of any sector is the sector number.

NOTE: Since the TEST command formats the disk, a scratch disk should be used before giving the command.

6.5.5 Buffer External Transfer Commands

Two Buffer Transfer Commands provide for transferring data from the buffer to external memory and from external memory to the buffer.

Buffer to External Memory Transfer Command. Upon receiving this command, the DMA is set up to transfer the RAM buffer data to the external memory. When the terminal count is reached, the controller posts the status and interrupts the System Processor if specified in the IOPB.

External Memory to Buffer Transfer Command. The DMA is set up to receive the data from external memory to RAM buffer. The operation is similar to the buffer to external memory transfer command.

6.6 DISK OPERATIONS

The diskette is the final destination or the source during the transfer of data between the external main system memory and a selected diskette. The data that enters the controller board from the system memory is in parallel format; the data that moves between the controller board and the selected disk drive is in serial format. This serial data is recorded on the selected diskette using frequency modulation (FM) format for single density mode or modified frequency modulation (MFM) format for double density mode. The track and sector format organization is shown in Figure 6-15.

The standard diskette is physically organized into 77 concentric tracks; in addition, it has an index hole which serves as a physical timing mark. These tracks are logically organized into sectors which may be of different lengths; however, each track must contain sectors of the same length. A mini diskette, on the other hand, contains 35 tracks which are also organized into sectors. Like the standard diskette, the length of the sectors can vary, but a given track must have sectors of the same size.

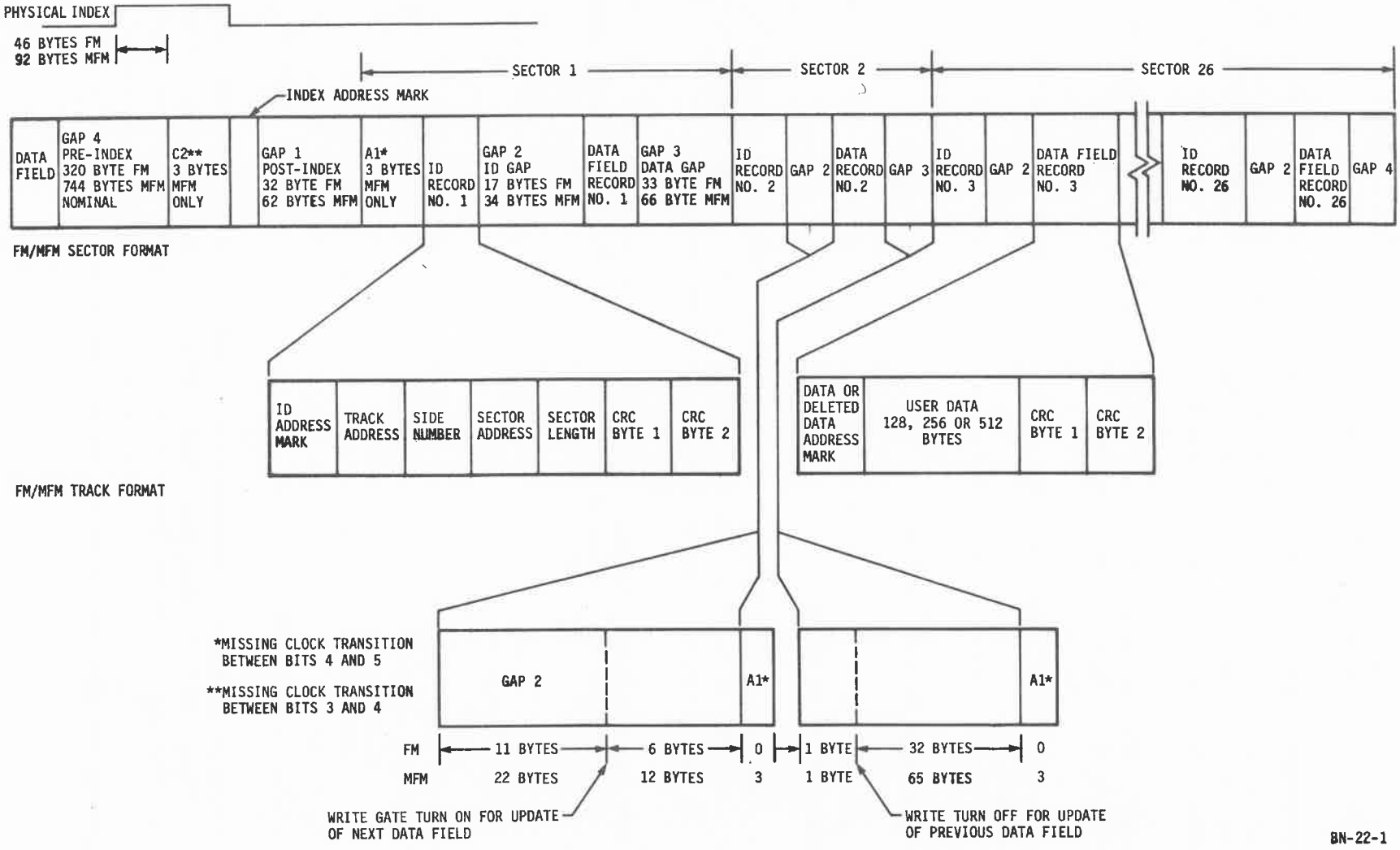


Figure 6-15 IBM FM/MFM Track and Sector Format

6.6.1 Track and Sector Format

Track Format. The signal that is termed the physical index results from the index hole on the diskette. When the index hole passes a light source on the disk drive it causes the generation of the index signal which, on its negative transition, marks the beginning of the track. Shown in Figure 6-15 are the first, second, and twenty-sixth (last) sectors. As shown, these sectors are separated from one another by gaps which contain no data. The index address mark is the actual beginning of the track and gap four is the ending.

Sector Format. The diagram in Figure 6-15 shows the format of the sector. All sectors are formatted in the same manner. The two basic elements are the identification (ID) and data fields. The ID field contains the track number, sector number, and the length of the sector. The data field of 128, 256 or 512 bytes in length, contains data that was stored during a data transfer. This data field is preceded by a data address mark, one byte in length.

6.6.2 Gap Configurations

Gaps of varying lengths separate the fields on a track. These gaps provide the important means of allowing the updating of individual fields without affecting adjacent fields. There are four different kinds of gaps as follows:

Post-Index Gap. This gap, called gap 1, comprises the bytes between the index address mark and the ID address mark of sector 1. The length of this gap is fixed and, therefore, not affected by any updating process. The gap is made up of 26 bytes of FF and 6 bytes of 00 (32 bytes for single density) and 50 bytes of 4E and 12 bytes of 00 (62 bytes for double density).

ID Gap. This gap, called gap 2, comes between the ID field and the data field. As defined, this gap comprises 11 bytes of FF and 6 bytes of 00 (17 bytes for single density) and 22 bytes of 4E and 12 bytes of 00 (34 bytes for double density).

Data Gap. This gap, designated gap 3, separates the end of the data field from the next ID field. It comprises 27 bytes of FF and 6 bytes of 00 (33 bytes for single density) and 54 bytes of 4E and 12 bytes of 00 (66 bytes for double density).

Pre-Index Gap. Designated gap 4, this gap is located between the last data field on the track and the index address mark. Gap 4 is 320 or 744 bytes in length. Several factors may cause the length of this gap to vary; such as the tolerances in write frequency, disk speed, or the updating of the data field in sector 26.

6.6.3 Address Mark Configurations

The address marks are unique bit patterns, one byte in length, that identify a particular field of information on a track. The following paragraphs discuss the four types of address marks.

Index Address Mark. The index address, a fixed number, begins each track. It is located between gap 4 and gap 1. The diagram in Figure 6-16 shows the format of this address mark.

ID Address Mark. The ID address mark begins each sector on a track; it is located between gap 1 and gap 2. The diagram in Figure 6-17 shows the format of this address mark.

Data Address Mark. The data address mark begins each non-deleted data field; the format of this address mark appears in Figure 6-18.

Deleted Data Address. This address mark appears at the beginning of each deleted data field, indicating that the field has been deleted. The diagram in Figure 6-19 shows the format of this address mark.

6.6.4 Cyclic Redundancy Check (CRC) Bytes

When the controller board writes a field on a diskette, it appends two CRC bytes to the field. These CRC bytes provide a means of checking for errors when the controller board reads this information back from the diskette. These two CRC bytes are generated from a permutation of the data bits, starting with bit zero and ending with bit 7 of the last byte in the field. This does not include the CRC bytes. The cyclic permutation is the remainder of the division of the data bits in the field by a generator polynomial. This generator polynomial is represented by the term G(X). It is derived by using the following equation: $G(X) = X^{16} + X^{12} + X^5 + 1$.

When the controller reads a field back from a diskette, the data bits are divided by the generator polynomial. A remainder of zero indicates that there is no error present; any other remainder indicates an error.

6.6.5 Formatting Considerations

The firmware supports variations in sector length and sequential and non-sequential sector format. When considering the transfer of data using double buffering, the user is advised to use sequential formatting for a maximum transfer which will gain the user savings in transfer times. Details of the software operation for formatting considerations and buffering transfer commands are given in Section 6.5.

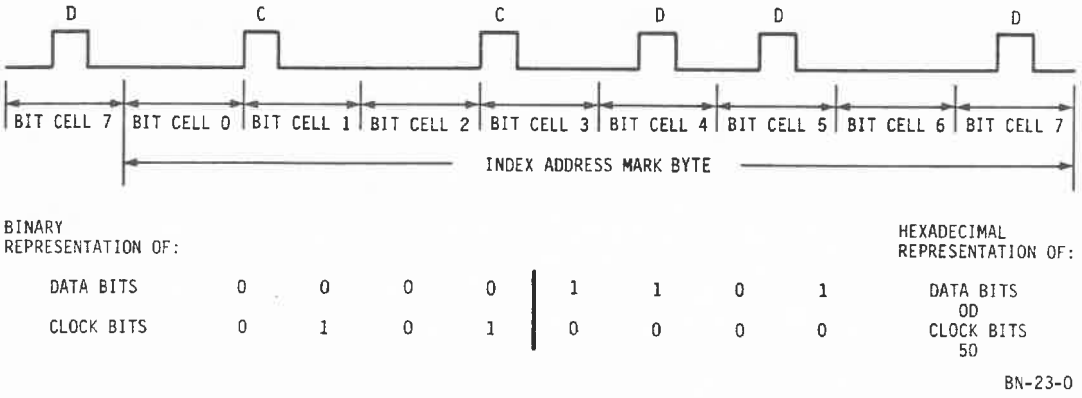


Figure 6-16 Index Address Mark)MFM)

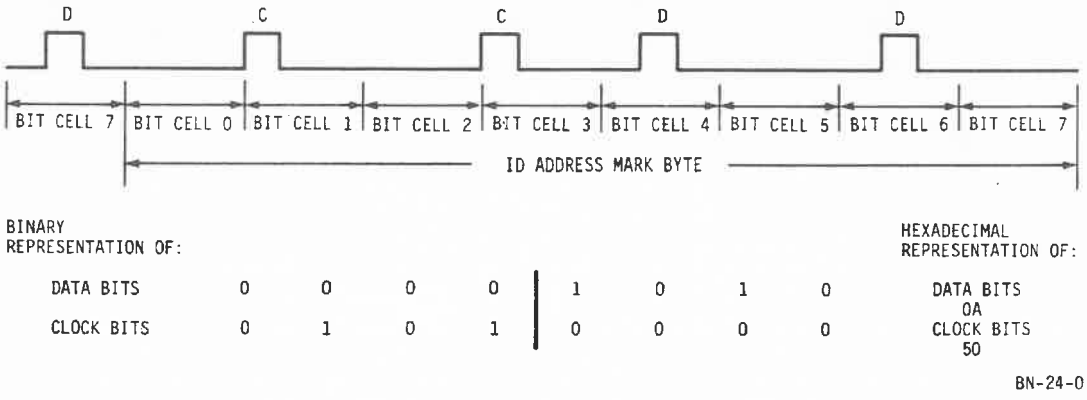


Figure 6-17 ID Address Mark (MFM)

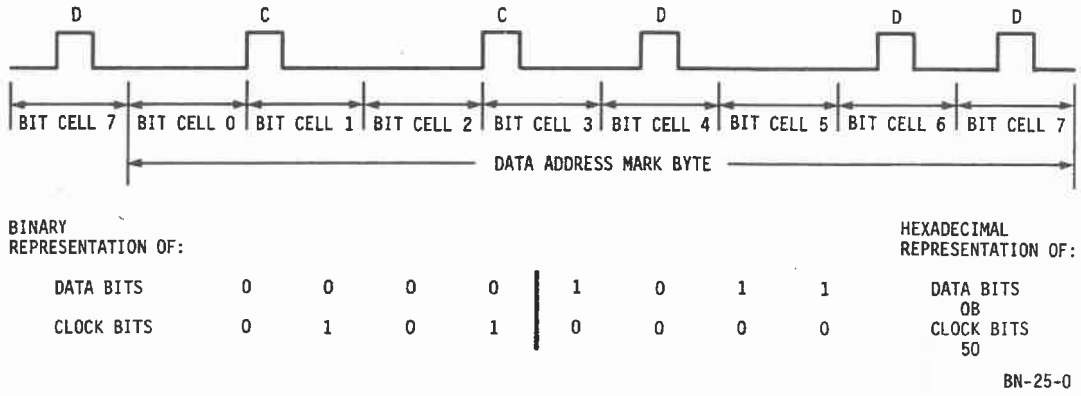

D C C D D D
BIT CELL 7 BIT CELL 0 BIT CELL 1 BIT CELL 2 BIT CELL 3 BIT CELL 4 BIT CELL 5 BIT CELL 6 BIT CELL 7
DATA ADDRESS MARK BYTE
BINARY REPRESENTATION OF:
DATA BITS 0 0 0 0 1 0 1 1
CLOCK BITS 0 1 0 1 0 0 0 0
HEXADECIMAL REPRESENTATION OF:
DATA BITS 0B
CLOCK BITS 50
BN-25-0

Figure 6-18 Data Address Mark (MFM)

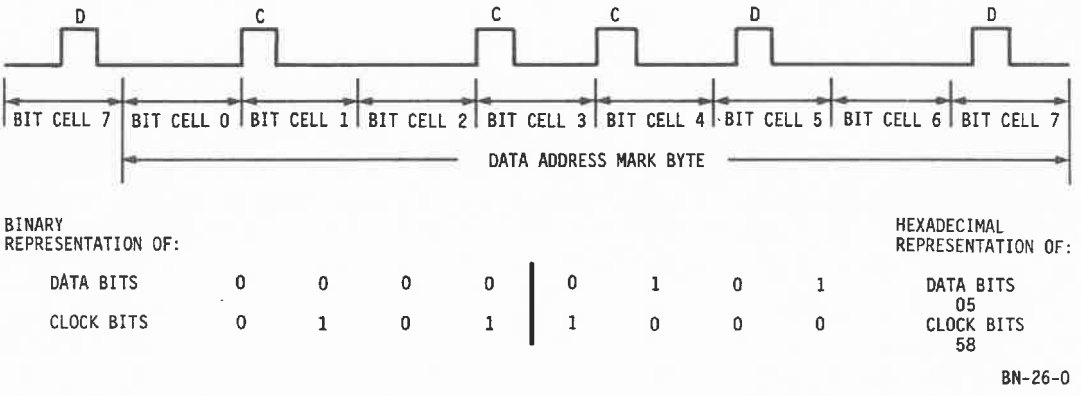

D C C C D D
BIT CELL 7 BIT CELL 0 BIT CELL 1 BIT CELL 2 BIT CELL 3 BIT CELL 4 BIT CELL 5 BIT CELL 6 BIT CELL 7
DATA ADDRESS MARK BYTE
BINARY REPRESENTATION OF:
DATA BITS 0 0 0 0 0 1 0 1
CLOCK BITS 0 1 0 1 1 0 0 0
HEXADECIMAL REPRESENTATION OF:
DATA BITS 05
CLOCK BITS 58
BN-26-0

Figure 6-19 Deleted Data Address Mark (MFM)

6.6.6 Miniature Disk Considerations

Miniature disk drives do not provide "Disk Change" status information and therefore are treated differently in the Idle Loop than standard drives.

In the Idle Loop, the drives are polled to check the READY status of the drives. If there is any change in the drive status, the miniature motor is turned on for a few milliseconds to move the index hole to eliminate the possibility of an erroneous status, after which the drive status will be updated.

However, in the Idle Loop, one type of drive status change cannot be determined; e.g., if the disk is inserted in the drive with the index hole aligned, and the previous status indicated the drive was not ready, the drive status will not be detected.

The System Processor can send the command for an unready drive. If the drive is not ready, the controller board will send not ready status and will not process the IOPB. But, if that drive was sensed as not ready because the index hole aligned, the IOPB will be processed.

Chapter 7

USER ADD-ON EQUIPMENT

7.1 GENERAL INFORMATION

The 6600 System is configured to support: a CRT Terminal device, a parallel Centronics printer interface, and a series RS232C interface. The system configuration consists of: hardware (drivers, receivers, jumpers), internal and external cabling, firmware routines, diagnostic programs, operating system support, and utility program support.

The following paragraphs provide reference information on the configuration and system support which is provided for these device interfaces. Reference should be made to Appendices B, C, and D for jumper location, assembly drawing, and schematics for the System Processor Board. Reference should be made to the System Software Reference Manual for specifics on the BIOS within the CP/M Operating System.

7.2 HARDWARE CONFIGURATIONS

7.2.1 CRT Serial Port

JUMPER	SIGNAL/FUNCTION
W17 4-8	Clear To Send
W17 5-9	Received Data
W17 6-10	Data Set RDY
W16 1-2	Clear To Send
W23 1-2	Request To Send
W22 6-7	Baud Clock #2
W22 2-3	Baud Clock #2
W6 3-4	Request To Send
W6 1-2	Data Terminal RDY
W3 1-2	Transmitted Data
W24 13-29	Interrupt #1
W24 9-19	Interrupt #2

Ref. Designator	Part No.
U25	DS1488
U15	DS1489
U16	DS1489

7.2.2 RS232C Serial Port

JUMPER	SIGNAL/FUNCTION
W10 4-8	Clear To Send
W10 5-9	Received Data
W10 6-10	Data Set RDY
W11 1-2	Clear To Send
W13 1-2	Request To Send
W21 6-7	Baud Clock #1
W21 2-3	Baud Clock #1
W5 5-6	Request To Send
W4 1-2	Data Terminal RDY
W5 4-7	Transmitted Data
W24 14-24	Interrupt #0
W24 10-20	Interrupt #4

Ref. Designator	Part No.
U22	DS1488
U13	DS1489
U14	DS1489

7.2.3 Centronics Printer Port

JUMPER	SIGNAL/FUNCTION
W7 1-2	Port E4 Input
W7 9-22	Data 0
W7 10-23	Data 1
W7 11-24	Data 2
W7 12-25	Data 3
W7 8-21	Data 4
W7 7-20	Data 5
W7 6-17	Data 6
W7 5-18	Data 7
W7 3-16	Gate 0
W7 4-17	Gate 1
W24 8-18	Interrupt #6

Ref. Designator	Part No.
U3	8303
U5	7408
U4	7408
U6	7438
XU7	——

7.2.4 Unassigned Parallel Port

JUMPER	SIGNAL/FUNCTION
W9 1-2	Port E8 Input
W9 9-20	Data 0
W9 10-21	Data 1
W9 11-22	Data 2
W9 12-23	Data 3
W9 8-19	Data 4
W9 7-18	Data 5
W9 6-17	Data 6
W9 5-16	Data 7
W24 7-17	Interrupt #7

Ref. Designator	Part No.
U8	8304
U10	BLC-902
U9	7438
U11	7438
U12	7438

7.3 FIRMWARE/SOFTWARE CONTROL

7.3.1 Boot Firmware

- Initializes CRT serial port through auto-baud routine. (110, 300, 600, 1200, 2400, 4800, 9600 baud supported.)
- Tests data bits within Centronics printer port.
- Does not initialize or test RS232C serial port or unassigned parallel port.

7.3.2 Diagnostics

- Tests CRT serial port through 'CRT' test program.
- Tests RS232C serial port through 'SERIAL' test program.
- Tests Centronics printer port through 'CENPTR' test program.

7.3.3 Basic I/O System (BIOS) within CP/M Operating System

- Supports CRT serial port as 'CRT' device.
- Supports RS232C serial port as 'TTY', 'PTP', and 'PTR'.
- Supports Centronics printer port as 'LPT' device.
- Does not support unassigned parallel port.

7.3.4 Utilities

- Supports Centronics printer port with 2 utility programs 'CEN80' and 'CEN132', which provide 80 and 132 character per line capability for the model 150 printer.

7.4 EXTERNAL CABLES

Two external cables, as indicated below, are offered by NSC which enable the connection of a CRT terminal device and/or a Centronics printer to the 6600 System.

- RS232 Cable (Six foot, twisted pair), P/N 970306571-001.
- Centronics Printer Cable (Twelve foot, Twisted pair), P/N 970306556-001.

7.5 SUPPORTED PERPHERALS

- CRT Terminal
  EIA RS232C Interface
  Baud Rate (110, 300, 600, 1200, 2400, 4600, 9600)
  Parity (ODD-OFF, EVEN-OFF, 0 or 1 - ON)
  Full Duplex Mode
  Auto Line Feed

- Centronics Printer
  Model 702 or equivalent
  Parallel Interface
  Auto Line Feed Disabled
  Character Set - 96
  Audio Alarm

  Model 150
  Parallel Interface
  Auto Line Feed Disabled

Chapter 8

SYSTEM MAINTENANCE

Field maintenance of the MICROSYSTEM 6600 is limited to replacement of the System Processor board, other BLC printed circuit boards, or other major subassemblies, such as the diskette drive module. The diagnostic software provided with the system allows thorough testing of the boards and diskette drive access. Voltage checks allow rapid isolation of possible power supply faults. Diagnostic procedures, designed to detect and clear "soft" diskette drive errors, eliminate unnecessary drive replacement.

The remainder of this chapter is divided in two sections. The first provides maintenance information for the microcomputer module. This section provides detailed information on using the diagnostic tests to detect faulty boards. Power supply checks are also provided.

The second section deals with the diskette drive module. In addition to power supply checks, drive diagnostic procedures are given.

Maintenance of optional peripherials, such as terminals and printers, should be performed following the precedures recommended in the manufacturer's manuals.

The 6600 diagnostics provide the user with a comprehensive set of programs to test and diagnose the system components. They are designed to allow the user to determine whether a malfunction is caused by a programming error or a malfunction in the system hardware.

These diagnostics are to be used on a 6600 system with standard, unmodified configuration. The diagnostics assume a mass storage device with the same interface as the BLC-8222 Double/Single Density Controller board.

Functionally, the diagnostics are divided into two parts: 1) The Boot PROM Diagnostic and Loader contained in the processor board on-board PROM, and 2) the Diagnostics system programs contained on the 6600 Diagnostic Diskette. Both of these groups are discussed in the following section.

8.1 MICROCOMPUTER MODULE MAINTENANCE

Before starting power supply checks or diagnostic tests, the microcomputer module should be given a thorough visual inspection to ensure problems are not mechanical in nature. Checking that boards are properly seated in the card cages, cable connectors are tight, and rear-panel connectors are in place, can eliminate many problems, especially those of an intermittent or random nature.

8.1.1 Power Supply Checks

Voltage checks on both the BLC-635 and BLC-665 power supplies can be performed with any quality analog or digital multimeter having a minimum of 20 kOhms/volt sensitivity. Checks should be made at the card cage power supply connectors. The connectors should be removed from the card cage to prevent erroneous readings due to loading effects.

DC power is provided to the card cages through two connectors, labeled P6 and P8. Figure 8-1 shows the P6 and P8 power connectors for both the BLC-635 and BLC-665 power supplies. Table 8-1 lists the expected voltage readings. If the correct readings are obtained with the connector removed from the card cage, replace the connector and recheck the voltage readings.

8.1.2 Boot PROM Diagnostic And Loader

The Boot PROM Diagnostic and loader in addition to containing a system loader program contains a PROM Monitor and a sequence of diagnostics which test the following areas:

- CPU
- Interval Timer and Interrupt Controller
- Parallel Input/Output
- Memory Map
- System Memory
- Floppy Disk Controller

The Boot PROM Diagnostic and Loader are in address locations 0000H to 07FFH (PROM). When the system is powered up or RESET the Program Counter is set to 0000H, thus invoking the Boot PROM Diagnostic. If no errors are detected, the Boot PROM Loader loads the loader program from diskette as described in Section 4.6.3.

There are two entry-points in the Boot PROM for user programs to return control if necessary.

Location 07F2H for non-error type of returns
Location 07F5H for loading-error returns

8.1.2.1 PROM MONITOR

The PROM Monitor is a seperate piece of code in the Boot PROM program and it is a mini-debugger. Control is transferred to the monitor routine if the user invokes it. The monitor is invoked by typing a upper case Z on the terminal, after the 'Mount System Disk And Hit Return Key' message has been displayed.

TABLE 8-1 BLC-635, -665 AC INPUT AND DC OUTPUT CONNECTORS

PIN NUMBER	INPUT	INPUT	INPUT	P6 OUTPUT	P8 OUTPUT	J3 OUTPUT
1	115	230	---	Ground	Key	+5V Unreg
2	115	---	---	+5 Volts	Ground	-5V Unreg
3	115R	---	100R	+5 Volts	-5 Volts	+12V Unreg
4	115R	230R	100R	-12 Volts	+12 Volts	Ground
5	---	---	100	---	+5 Volts	"AC Low"
6	---	---	---	Ground	+5 Volts	---
7	---	---	---	Key	Ground	Key

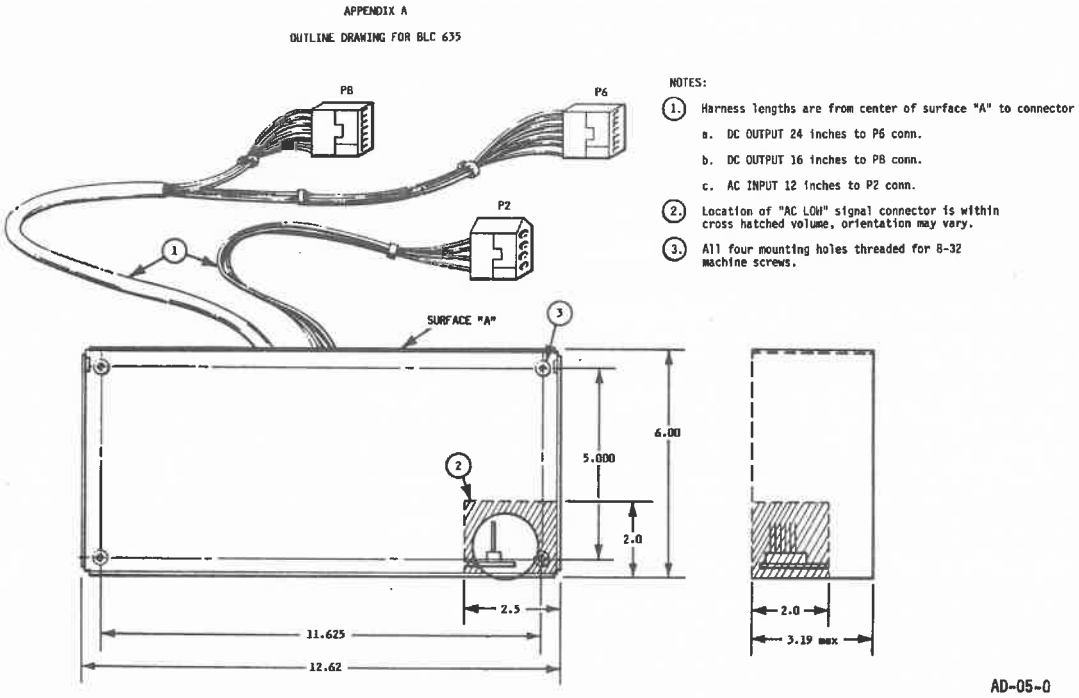


Figure 8-1 BLC-635, -665 DC Power Connectors

The PROM Monitor provides the following commands:

B Boot system or diagnostics.
The B command will attempt to boot from disk even if there was a diagnostic error.

C Change value of memory locations.
The form of the change command is

C <address>

After typing the address, the space key causes the monitor to print the contents of the current address and prompt with a '=' for alteration to this location. Typing return after the optional new data terminates the command. Typing a space increments to the next location.

L Load memory from serial port.
The form of the command is

L <optional address displacement>

(echoed to selected device). The Load format is:

Byte 0	Record Mark = ':'
Byte 1,2	Record Length <= 256 If record length = 0 load terminates.
Byte 3-6	Load address if record type = 00 Start address if record type = 01 Stack pointer if record type = 02
Byte 7,8	Record Type 00 = Data 01 = Terminate load and run at start address 02 = Stack pointer record

Byte 9 to Last Data (ASCII HEX)

Last Byte Checksum

A good load terminates with 'return, linefeed, #'. A bad load terminates with 'bell, return, linefeed, #'.

Typical Records:

```
:05B0000010B0CD0578XX          - Data Record
:09B00600203015251317F319EDXX  - Data Record
:ZZF00002XX                    - Stack Pointer
:ZZB00001XX                    - Start Address
```

Note: ZZ = Don't care if non-zero
XX = Checksum

G Run program from <address>.
The form of this command is

G <address>

The user program must end with a RESTART 1 op-code (C7H).

R Change register pair values.
The form of the change register command is

R <register pair>

After typing the register pair a space key causes the monitor to display the contents of the current register pair and prompt with '=' for alterations. Pressing RETURN after the optional new contents terminates the command. Typing a space displays the contents of the next register pair.

NOTES: 1. When using the G command, the user program must exit with the IX register restored to its original value.

2. The R command can not change the Z80 alternate registers.

3. When the system RAM diagnostic passes, the memory available to the user is from 1000H to 107FH, 5000 to 507FH, and E000 to FFF0H.

4. In case of Error 11 or 12 (memory failure), the monitor results are not guaranteed because the user registers could be stored in the system memory where the failure occurred.

8.1.2.2 CPU Diagnostics

The CPU Diagnostics are designed so that a small subset of instructions and registers are tested first. These are then used to test another subset of instructions and registers. This building up of tested instructions and registers is continued until the set of instructions needed to load a program has been tested. The set consists of the following classes of items.

- All registers
- Compare instructions
- Unconditional and conditional jumps
- Increment and Decrement instructions
- Load instructions
- Rotate instructions
- Arithmetic instructions
- Stack operations
- Bit set and reset instructions
- I/O instructions

Each register is tested for all bits set and reset. Jumps are tested for both successful and failed conditions. Increment and Decrement instructions are tested concurrently with the above tests and are used to change values of the registers. Load instructions are restricted to register-to-register and memory-to-register. Rotate and arithmetic instructions use only PROM memory data and registers. Stack instructions are tested after the RAM memory test described in Section 8.1.2.4 has been passed.

Following is a list of the tested instructions:

LD
ADD, SUB, XOR
INC, DEC
RLCA, RLA, RRA
AND, OR, CP
PUSH, POP, CALL, RET
JZ, JNZ, JR NZ, JR Z

Whenever an error occurs, an error message is generated and prompts the user to mount a diskette if it is not present.

8.1.2.3 PROM Checksum

Once the first subset of instructions are checked, the Boot Firmware determines if the checksum is correct. If there is an error, the Boot Firmware sends a mesage to the CRT serial port. After an error message, the Boot Firmware will try to load a diskette or else it will prompt the user to mount a diskette.

8.1.2.4 System Memory Diagnostics

Memory areas of either 4K or 80 bytes in size within the 64K bytes of system memory have a 55H and AAH written to it. The memory is read and the value compared for both data patterns to verify the memory contents.

The segments tested are:

1000 - 107FH
5000 - 507FH
D000 - DFFFH
E000 - EFFFH
F000 - FFFFH

If this test fails, an error message is generated. The program then prompts the user to mount a diskette if it is not installed.

8.1.2.5 Interval Timer and Interrupt Controller Diagnostics

Both the Interval Timer and Interrupt Controller are tested to verify their basic operations. If either (or both) fail, an error flag is set. If the interval timer does not work, intelligent messages can not be displayed on the CRT.

For the interval timer, all counters are tested in the binary operation. Counter 0 interrupts the CPU after appoximately 50 microseconds. If an interrupt is not received by the CPU in the specified amount of time, then either the interrupt controller or interval timer is not working properly. Counter 0 is read to determine if it has counted down to zero. If the value read is zero the interrupt controller is in error. If the value read is not zero the interval timer is in error.

Upon receiving an interrupt, counters 1 and 2 are read. If the counts are not between the specified limits the interval timer is incorrect.

NOTE: Only the master interrupt controller is tested by the boot firmware. The slave interrupt controller, which interfaces to MULTIBUS devices, is tested by the diskette based system diagnostics.

8.1.2.6 Parallel I/O Diagnostics

The parallel port, which is used to interface to the Centronics Printer, is tested. However, signals which would cause some printer action are not tested. Data patterns of 55H and AAH are used.

If an error occurs, a message is sent to the CRT.

The second parallel port, which is unassigned, is not tested because its configuration and possible device interaction is user application dependent.

8.1.2.7 Memory Map Diagnostics

Each of the sixteen memory map locations, located at I/O port D7 Hex, are set to 55H and AAH.

The values written are read back to verify the map contents for each value. Any instructions needed to implement this test will be verified before the actual invocation of the test.

If an error occurs, an error message is sent to the CRT.

8.1.2.8 Floppy Disk Controller Diagnostics

Port 71 is read until either 1.1 seconds has passed, indicating an error, or bit 7 is off, indicating the Floppy Disk Controller is not busy. Then the diagnostic results are read from Port 70, which has the following format:

bit 7 = 1 or 0 if diagnostic results are posted or invalid.
bit 6 = 0 always.
bit 5 = 1 or 0 if controller-chip test passed or failed.
bit 4 = 0 always.
bit 3 = 1 or 0 if scratch memory test passed or failed.
bit 2 = 0 always.
bit 1 = 1 or 0 if checksum test passed or failed.
bit 0 = 0 always.

Then Port 72 is read to determine the type of board and drive configuration, according to the following format:

bit 7 = don't care.
bit 6 = 0 always.
bit 5 = don't care.
bit 4 = 0 always.
bit 3 = 1 or 0 if heads-per-drive equals 1 or 2.
bit 2 = 1 or 0 if drive-type is mini or standard.
bit 1 = don't care.
bit 0 = 1 or 0 if board is dual-density or single-only.

The data from Port 72 is saved in register B when the Boot Firmware passes control to the Boot Loader, loaded from Track 0, Sector 1.

If an error occurs, an error message is generated that prompts the user to mount a diskette (if it is not already installed).

8.1.2.9 Auto Baud Control

The Microsystem 6600 will support terminal devices with the following Baud rates:

1. 9600
2. 4800
3. 2400
4. 1200
5. 600
6. 300
7. 110

The user invokes the Baud rate setting by striking the RETURN key repeatedly.

If there is no response 10 seconds after the RETURN key is hit, there is a failure which cannot be detected by the firmware.

NOTE: The system terminal device must be connected to the serial port labeled CRT. The second serial port, labeled RS232C, is not supported by the Boot Firmware.

Error Handling

When an error occurs in any of the above tests, a flag is set in the firmware to indicate the error, and the following message is sent to the CRT.

ERROR xx

where xx is one of the error numbers listed in Table 3-1.

NOTE: An error terminates any furthur diagnostic testing.

8.1.3 Diagnostic Diskette

Chapter 3, Section 3.7, covered the loading, boot PROM errors, and general operation of the diagnostic software provided with the MICROSYSTEM 6600. This section covers the purpose of the diagnostic tests on the Diagnostic Diskette, lists the subtests, describes optional operating procedures, and gives error handling procedures. Error handling procedures include error message format, error recovery, and fault isolation.

Currently, the diagnostic software provides six major test routines. They are:

- CPU test
- Memory test
- Diskette drive test
- CRT test
- Printer test
- Serial port test

These tests, along with the diagnostic monitor, are described in the following subsections.

8.1.3.1 Diagnostic Monitor

The Diagnostic Monitor Program (DM) is a diskette-resident diagnostic operating system. It serves as an intelligent communication medium between the operator and the test programs. The Diagnostic Monitor Program has the following features and functions:

- Loads the test programs in absolute object format from the diskette into RAM and checks whether the loading is completed correctly.
- Contains the keyboard interface routine for selecting and running of tests.
- Outputs all printouts via routines in the monitor. All printouts are sent to the system CRT until the operator intervenes and selects either the CRT or the Printer.
- Under operator control, re-run a subtest a specified number of times or continuously until halted by the operator.
- Under operator control, strings all device tests to be run sequentially.
- Provides general purpose subroutines that are used by all the test programs.

Load Procedure

The DM is loaded via the Bootstrap Loader Program resident in PROM. The procedure for loading is as follows.

a. Insert the diagnostic floppy disk in either drive.

b. Momentarily press the RESET switch on the microcomputer module.

c. At the terminal, repeatedly strike the RETURN key.

d. The following message will be displayed on the CRT:

```
Z6600 Diagnostic Monitor    Version n.n    mm/dd/yy
COPYRIGHT© 1981, National Semiconductor Corporation,
All Rights Reserved

Command    Parameter          Comment

  DE       ALL/CRT/LPT        Select listing devices
  ME       ALL/ ERROR         Select type of message
  OP       ---                Display options selected
  RE       O/N                Repeat infinitely/n times
  RU       ---                Run
  SU       AU/N/ALL           Select subtest
  TE       ALL/XXXXXX.BIN     Select test

Enter commands
>
```

Operating Procedure

The normal operating procedure is to run all the automatic subtests on all the permanent system replaceable modules as shown in the following example:

Example:

```
ENTER COMMANDS
>RU (CR)
CPU          VERSION n.n    mm/dd/yy          LOADED
.
.
.
ENTER COMMANDS
>
```

where (1) (CR) means the Carriage Return key.
(2) Operator inputs are underlined and the system responses are not.
(3) CPU is the test program name of the first test program.

All the automatic subtests in each test program are loaded, run, and their outputs are sent to the CRT. A message is printed at the end of each subtest indicating whether it passed or failed. In the case of subtests which have to be visually checked (as for the Printer) an EXITED message is printed instead of a pass/fail message. When the last subtest in each test has been run, the next device test program is loaded automatically and the whole cycle repeats as in the first device test. Table 8-2 provides a list of device test programs, their names, and the sequence in which they are run.

In addition to the normal operating procedure described above, the user may choose an optional operating procedure. Table 8-3 lists all the commands available in the Diagnostic Monitor. The operator can select the option according to his needs by keying in a sequence of commands after the enter command prompt message (>) is printed on the CRT. Each command is represented by two characters, followed by a space, followed by an optional parameter and a carriage return. The last command must be the RU command. Table 8-4 summarizes the Keyboard entries common to all disgnostic tests.

The example below shows the normal loading of an individual test:

Example:

```
ENTER COMMANDS
>TE CPU (CR)
>RU (CR)
CPU          VERSION n.n    mm/dd/yy          LOADED
.
.
.
```

The underlined characters are entered by the operator. In the above example, the test program has been loaded and started. Results are displayed as they occur.

TABLE 8-2 CONTENTS OF THE DIAGNOSTIC FLOPPY DISKETTE

PROGRAM NAME	DESCRIPTION	EXECUTION SEQUENCE
6600.DM	Diagnostic Monitor	
CPU	Processor Test	1
MEMT1	Memory Test Part 1	2
MEMT2	Memory Test Part 2	3
CRT	CRT Test	4
CENPTR	Centronics Printer Test	5
FLOPPY	Floppy Disk Test	6
SERIAL	RS232C serial port	7

Execution sequence is the order in which device test programs are loaded and run under the normal loading procedure by the DM.

TABLE 8-3 DIAGNOSTIC COMMAND TABLE

MNEMONIC	PARAMETER	FUNCTION	DEFAULT (When Loaded)
DE	CRT/LPT/ALL	Select output device, CRT or LPT	Both
ME	ERROR	Message output by test program can choose to print errors only	All Messages
OP	-----	Display currently running options	-----
RE	nnnnn	Repeat a subtest/test	Once
RU	-----	Run	-----
SU	n/ALL/AU	Select subtest(s)	All subtests
TE	XXXXXX	Specify test desired	All device tests listed in Section 8.1.2

TABLE 8-4 KEYBOARD INPUT COMMAND STRUCTURE

KEY	FUNCTION
>	The greater-than symbol (>) is displayed on the CRT and/or the printer to indicate that the program is waiting for a user input.
(CR)	A carriage return (CR) must be typed to end every command input.
DEL	If, during command entry, an error is made, it can be deleted by the use of the "DEL" key to delete the previous character. A string of n characters can be deleted by pressing the "DEL" key n times.
ESC	The "ESC" key is used to exit from the currently running subtest and return to the command interpreter.
NOTE:	If an invalid entry has been made, i.e., program name or subtest number that does not exist, the bell is rung and an error message is printed.

To run all of the subtests for all of the tests without running each test individually enter the following commands:

```
Enter Commands
>SU ALL (CR)
>RU (CR)
XXXXXX          Version  n.n    mm/dd/yy          LOADED
.
.
.
Enter Commands
>
```

DM Load Error Detected by the Bootloader

If a load error occurs during the load of the Diagnostic Monitor Program, the following message sequence will appear:

```
6600.DM load error
```

NOTE: If the Diagnostic Monitor has been loaded and run then the results are unpredictable, therefore, a reload should be attempted, possibly through a different disk drive.

Test Program Load Errors Detected by DM

If a load error occurs during the loading of a Test Program the following message will appear:

```
Checksum error (XXH) found
```

where XX is the checksum value in hex.

The test program has been loaded and run, but the results are unpredictable; therefore, a reload should be attempted. Depress the RESET switch and reload by hitting RETURN key.

If a Test Program is requested that does not exist, the bell is rung and the following message is printed:

```
XXXXXX.XXX - file not found
Enter commands
>
```

Processor and Memory Errors Detected by DM

The DM performs memory tests for the 16K area (4000-7FFFH) reserved for the individual Test Programs. If an error is detected in this area, the following error message will be printed.

6600.DM memory error at XXXX: expected YY is ZZ

where XXXX = memory location in Hex
YY = expected hex pattern
ZZ = actual content of XXXX

Basic instructions used by DM program that have not been verified by the Bootstrap Loader are tested immediately upon initialization of the monitor. If an error is detected, the DM prints the following message.

DM CPU instruction error

Command Input Error Detected by DM

If a syntax error is detected in the keyboard command, for example, a nonexisting command, the DM prints a message as below:

```
Invalid entry
>
```

Retype the correct input.

Device Error Detected by DM

If during testing, a hardware error has been detected by the DM on either the CRT, Floppy or Printer, one of the following messages will be printed.

CRT error	(e.g. illegal function code found)
Disk error	(e.g. disk not ready)
Printer error	(e.g. out of paper or no printer attached)

Errors Detected by Device Test Program

1. If an invalid subtest number has been selected, after the loading, the DM will check again to ensure subtest number selected is valid for a particular test program (each test program has a number which specifies the maximum subtest number contained in this module). The following message will be printed:

```
invalid subtest selected
.
.
Enter commands
>
```

2. Error messages from the test programs are in this format:

XXXXXX SUBTEST nnn ERROR mmm

where XXXXXX is the test program name, nnn is the subtest number, mmm is the error identification code. Refer to each test program section for the meaning of the error codes.

Error Recovery

If a recoverable error is encountered during subtest execution, the subtest will print the pertinent information (including an error message) and then continue. All other errors will cause the subtest to halt and hardware RESET is needed in order to run subtests individually (in sequence) again. The subtest can always be restarted by entering the appropriate commands.

8.1.3.2 System Processor Test

The purpose of this test is to fully test the Z80A microprocessor and associated peripheral devices located on the System Processor board. Table 8-5 lists the subtests.

NOTE: The peripheral devices, also located on the board, and associated with the CRT serial port, RS232C serial port, and printer parallel port, are tested by the use of the specific test programs developed for those devices and documented in Subsections 8.1.2.4 and 8.1.2.5. Also, the 24-bit unassigned parallel port is not tested by the diagnostic utility.

Normal Operating Procedures. All the required subtests will be run sequentially in a normal testing procedure through the commands entered. They are from subtest 1 to subtest 7. Figure 8-2 shows the expected results following normal operating procedures.

Optional Operating Procedures. Refer to Table 8-3 for a list of diagnostic commands. The following options are pertinent to CPU subtests.

The command options can be intermixed. The following self-explanatory examples apply to all of the subtests unless otherwise specified:

TABLE 8-5 SYSTEM PROCESSOR SUBTESTS

ATTRIBUTES AND FUNCTIONS
Subtest 1 (Required, Automatic) Data transfer test. All register to register moves done except memory to H, memory to L, L to memory, and H to memory.
Subtest 2 (Required, Automatic) Arithmetic test. Test all arithmetic instructions on all registers.
Subtest 3 (Required, Automatic) Logic test. Tests all logic instructions on all registers.
Subtest 4 (Required, Automatic) Branch, non-conditional test. All branch instructions will be tested.
Subtest 5 (Required, Automatic) Stack, machine control test. The rest of instructions will be tested except I/O test will not be performed and machine control instruction HLT will not be tested.
Subtest 6 (Required, Automatic) Tests the Z80 instruction/operand combinations that are not a part of the 8080 instruction set. Subtest 7 (Required, Automatic) Using a hardware timer and setting up an illegal I/O address, tests the fail safe timer.

```
ENTER COMMANDS
>TE CPU (CR)
>RU (CR)
CPU    Version  n.n    mm/dd/yy    LOADED

CPU SUBTEST 01 PASSED
CPU SUBTEST 02 PASSED
CPU SUBTEST 03 PASSED
CPU SUBTEST 04 PASSED
CPU SUBTEST 05 PASSED
CPU SUBTEST 06 PASSED
CPU SUBTEST 07 PASSED
ENTER COMMANDS
>
```

Figure 8-2 Expected Results For CPU Test Automatic Run (Normal Operating)

Example 1. Normal Testing

```
ENTER COMMANDS
>TE CPU (CR)
>SU NN (CR)
>RU (CR)
CPU    Version  n.n    mm/dd/yy    LOADED
   (subtest under testing)
CPU SUBTEST NN PASSED
ENTER COMMANDS
>
```

NOTE: NN = valid subtest number

Example 2. End a Subtest Before it is Finished

```
.
.
.
   (Same as in Example 1)
.
.
.
   (Test is running)
   (Press ESC Key)
CPU SUBTEST NN ENDED
ENTER COMMANDS
>
```

Example 3. Intermixing Commands Options

```
>TE CPU (CR)
>DE CRT (CR)                (select CRT as output media)
>ME ERROR (CR)              (error message only)
>RE 3 (CR)                  (repeat 3 times)
>SU NN (CR)
>RU (CR)
   (test starts running)
.
.
.
ENTER COMMANDS              (this will be printed when subtest NN
>                           is repeated 3 times and finished)
```

Error Recovery. If an error is encountered which is considered recoverable, the subtest will print the pertinent information and continue until an error message is printed. All other errors will cause the subtest to halt and hardware RESET is needed in order to run subtests individually (in sequence) again. The subtest can be restarted by entering the appropriate commands.

Error Message. When the subtest fails (status error, comparison error, etc.) an error message is printed. The error message consists of device name, a subtest number, and an error number as follows:

```
CPU SUBTEST NN ERROR MM
```

Where NN = subtest number
MM = error code

Refer to Table 8-6 for further details.

TABLE 8-6 SYSTEM PROCESSOR TEST ERROR TABLE

SUBTEST NUMBER	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
1, 2, 3, 4, 5, 6	ERROR 01 ERROR 02 ERROR 03 ERROR 04	- CPU instr. execution error - CPU reg. data pattern error - CPU stack pointer error - CPU status flag error	Replace System Processor Board
7	ERROR 19	- Fail safe timer 10 milli-second timing error	Replace System Processor Board

Fault Isolation. All subtests should be run in sequence to enhance the diagnostic capability. Subtests 1 thru 6 are designed to test the Z80 instruction set. Subtest 7 is designed to test the interval timer, in both binary and BCD modes. Subtest 8 is designed to test the master interrupt controller on the board. Subtest 9 is designed to test the fail-safe timer. Refer to Table 8-3 for test option descriptions.

8.1.3.3 Memory Test

The purpose of this test is to fully diagnose the system memory. This is accomplished in two tests, MEMT1 and MEMT2. Refer to Table 8-7 for a list of subtests.

Normal Loading Procedure. After the message "ENTER COMMANDS" a ">" should appear on the first column of the next line (Note: The ">" symbol indicates a key entry is required by the operator). The operator enters, via keyboard, the Test command followed by a space, the file name of the Memory test (MEMT1 or MEMT2), and a carriage return (CR). The operator then enters the RUN command to start the loading and executing. A self-explanatory example is given below:

Example:

```
ENTER COMMANDS
>TE MEMT1 (CR)
>RU (CR)
>MEMT1    Version  n.n    mm/dd/yy    LOAD
.
.
.
```

In the above example, the test program has been loaded and started. Any results will be displayed as they occur.

Normal Operating Procedures. All the required subtests will be run sequentially in a normal testing procedure through the commands. They are from subtest 1 to subtest 5. Figure 8-3 shows expected results during normal operating procedures.

Optional Operating Procedures. Refer to Table 8-3 for diagnostic commands. The following sections of options are pertinent to the Memory subtests.

The command options can be intermixed. The following self-explanatory examples apply to all of the subtests unless otherwise specified:

Example 1. Normal Testing

```
ENTER COMMANDS
>TE MEMT1 (CR)
>SU NN (CR)
>RU (CR)
MEMT1    Version  n.n    mm/dd/yy    LOADED
   (subtest under testing)
```

(continued on page 8-24)

TABLE 8-7 A BRIEF DESCRIPTION OF THE MEMORY TEST SUBTESTS

ATTRIBUTES AND FUNCTIONS
Subtest 1 (Required, Automatic) Quadrant decoder test. Write 01, 02, 03, and 04 to the four quadrants and read back to verify all four quadrants are being accessed.
Subtest 2 (Required, Automatic) Read/Write test. Fill the area under test with 00H pattern, then read back and compare. If mismatch has been found between expected data and received data, the error address and both data patterns will be printed on the output media. Repeat above test using FF, AA, and 55 patterns.
Subtest 3 (Required, Automatic) Address test. Fill the area under test with non-zero incrementing pattern (01H-FFH are used cyclically), then read and compare the pattern. If mismatch has been found, print out error address and both data patterns.
Subtest 4 (Required, Automatic) SKIPPAT test. This is a pattern sensitivity test, a predefined skip pattern is used to accomplish this test. NOTE: This test takes several minutes (3-7) to complete.
Subtest 5 (Required, Automatic) Retention (Refresh) test. Fill the area under test with 55H. Wait one minute and read back. Comparisions are made for proper contents. If mismatch has been found, print out error address and both received and expected data patterns.
NOTE: 1. Memory test 1 is loaded and run as other test programs. This test will test high RAM (location 8000H thru FFFFH). 2. Memory test 2 is loaded into high RAM (the area tested by memory test 1), and has the same subtest and functions as Memory test 1. This used to test low RAM (location 0000H thru 7FFFH).

```
ENTER COMMANDS
>TE MEMT1 (CR)
>RU (CR)
MEMT1    Version  n.n    mm/dd/yy    LOADED

MEMT1 SUBTEST 01 PASSED
MEMT1 SUBTEST 02 PASSED
MEMT1 SUBTEST 03 PASSED
MEMT1 SUBTEST 04 PASSED  — 3-7 minute
MEMT1 SUBTEST 05 PASSED
ENTER COMMANDS
>
```

NOTE: The above procedure is also applicable to Memory test 2. However, the filename MEMT2 must be entered in the TEst command.

Figure 8-3 Expected Results For Memory Test Automatic Run (Normal Operating)

```
MEM1 SUBTEST NN PASSED
ENTER COMMANDS
>
```

NOTE: 1. NN = Valid subtest number
2. MEMT1 can be replaced by MEMT2 to test lower 32K memory bank.

Example 2. End a Subtest Before it is Finished

```
.
.
.
   (Same as in Example 1)
.
.
.
   (Test is running)
   (Press ESC Key)
MEMT1 SUBTEST NN ENDED
ENTER COMMANDS
>
```

Example 3. Intermixing Commands Options

```
>TE MEMT1 (CR)
>DE CRT (CR)              (select CRT as output media)
>ME ERROR (CR)            (error message only)
>RE 3 (CR)                (repeat 3 times)
>SU NN (CR)
>RU (CR)
   (test starts running)
.
.
.
ENTER COMMANDS            (this will be printed when subtest NN
>                         is repeated 3 times and finished)
```

Error Recovery. If an error is encountered which is considered recoverable, the subtest will print the pertinent information and continue until error message is printed. The subtest can always be restarted by entering the appropriate commands.

Error Message. When the subtest fails (status error, comparison error, etc.) an error message is printed. The error message consists of test name, a subtest number, and an error number as follows:

```
MEMT1 SUBTEST NN ERROR MM    or
MEMT2 SUBTEST NN ERROR MM
```

Where NN = subtest number
MM = error code

Refer to Table 8-8 for further details.

TABLE 8-8 MEMORY TEST ERROR TABLE

SUBTEST NUMBER	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
1	EXPECTED DATA = XX, ACTUAL DATA = YY ADDRESS = HHHH ERROR 01	Quadrant latch test failed, where XX, YY, and HHHH are Hex numbers	Replace memory board
2	EXPECTED DATA = XX, ACTUAL DATA = YY ADDRESS = HHHH ERROR 01	Checkerboard test failed (00, FF, AA, 55 patterns used) at location specified	Replace memory board
3	EXPECTED DATA = XX, ACTUAL DATA = YY ADDRESS = HHHH ERROR 01	Address test failed at location specified	Replace memory board
4	EXPECTED DATA = XX, ACTUAL DATA = YY ADDRESS = HHHH ERROR 01	SKIPPAT test failed at location specified	Replace memory board
5	EXPECTED DATA = XX, ACTUAL DATA = YY ADDRESS = HHHH ERROR 01	Memory retention failed at location specified	Replace memory board

Fault Isolation. All subtests should be run in sequence to enhance the diagnostic capability. Subtest 1 is designed to test the quadrant selection. Subtest 2 is designed to test the read/write capability of all memory cells. Subtest 3 is designed to test the addressing lines. Subtest 4 is designed to test pattern sensitivity of the memory cells. Subtest 5 is designed to test the data retention capability of the dynamic RAM. Refer to Table 8-3 for test option descriptions.

8.1.3.4 CRT Test

The purpose of this test is to verify the functionality of both the RS232C serial port and the system CRT console device. Table 8-9 lists the subtests for the CRT test.

Normal Loading Procedure. After the message "ENTER COMMANDS" a ">" should appear on the first column of the next line (Note: The ">" symbol indicates a key entry is required by the operator). The operator enters, via keyboard, the TEst command followed by a space, the filename of the CRT test (CRT) and a carriage return (CR). The operator then enters the RUn command to start the loading and executing. A self-explanatory example is given below.

Example:

```
ENTER COMMANDS
>TE CRT (CR)
>RU (CR)
>CRT    Version  n.n    mm/dd/yy    LOAD
.
.
.
```

Where underlined characters are entered by the operator, and the digits after the filename are the version number and the release date for the CRT test program.

Load Error Procedure. If a load error occurs during the loading of the CRT test program, the following messages will appear:

```
CRT    Version  n.n    mm/dd/yy    LOADED
CHECKSUM ERROR (XXH) FOUND
.
.
.
```

The test program has been loaded and started, but a checksum error was found. Therefore, a reload should be attempted, possibly through a different diskette drive.

TABLE 8-9 BRIEF DESCRIPTION OF CRT TESTS

ATTRUBUTES AND FUNCTIONS
Subtest 1 - Character Set (Required, Manual) Transfer 94 printable ASCII characters to CRT, wait for operator to verify with specification.
Subtest 2 - Screen Linearity Test (Required, Manual) Fill screen with ASCII '0' except corner place Z's (last line, line 1, positions 1 and 80). The screen should have 4 Z's clearly visable at the corner. All 0's should be clear and evenly spaced over full screen. Example: Z000 - - - 000Z 0000 - - - 0000 - - - - - - - - - - - - - - 0000 - - - 0000 Z000 - - - 000Z
Subtest 3 - Bell Test (Required, Automatic) Sounds the bell ten times
Subtest 4 - Keyboard Test (Required, Manual) Read key and display. Instruct operator to depress every key on keyboard once (save 'Return' key for last as this will be the exit). The test is automatically exited on the 82nd character.

Normal Operating Procedures. All the required subtests - manual and automatic - will be run sequentially in a normal test procedure through the commands. They are from subtest 1 to subtest 4.

Subtests that required operator intervention must be accomplished through operator interaction. They are described below in detail:

Subtest 1 tests the CRT Character ROM. A character string will be outputed to CRT monitor in the following order.

```
! " # $ % 6 7 8 9 * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ? @
A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [ \ ]^ _ '
a b c d e f g h i j k l m n o p q r s t u v w x y z { ¦ }
```

Press RETURN Key to exit this subtest.

Subtest 2 tests Screen Linearity. The screen will be filled up by the following format:

```
Z000 - - - 000Z          Line 1
0000 - - - 0000
-  - - - - - -  -
-  - - - - - -  -
0000 - - - 0000
Z000 - - - 000Z          Last line
```

Press RETURN Key to exit this subtest.

Subtest 3 checks the bell. The bell will ring. If it is not heard the bell is not working properly. This subtest will exit automatically.

Subtest 4 tests the Keyboard. After the message, "PRESS ALL KEYS AND VERIFY WITH SPECIFICATION - EXIT BY "RETURN" KEY", is displayed on the screen, the operator should press EVERY key on keyboard at least once (save RETURN Key for last as this will be the exit). Each key should be properly echoed. Refer to Table 8-10, Code Assignments.

Figure 8-4 shows a display of the result for normal operating procedures.

Optional Operating Procedures. Refer to Table 8-3 for diagnostic commands. The following sections of options are pertinent to CRT subtests.

The command options can be intermixed. The following self-explanatory examples apply to all of the subtests unless otherwise specified.

TABLE 8-10 SYSTEM 6600 TERMINAL KEY CODE ASSIGNMENTS

KEY NAME	NORMAL	SHIFT	CONTROL	SHIFT/CONTROL
BACKSPACE	08	08	08	08
TAB	09	09	09	09
LINE FEED	0A	0A	0A	0A
RETURN	0D	0D	0D	0D
ESCAPE	1B	1B	1B	1B
SPACE	20	20	20	20
, (<)	2C	3C	2C	3C
- (=)	2D	3D	2D	3D
. (>)	2E	3E	2E	3E
/ (?)	2F	3F	2F	3F
0	30	30	30	30
1 (!)	31	21	31	21
2 (")	32	22	32	00
3 (#)	33	23	33	23
4 ($)	34	24	34	24
5 (%)	35	25	35	25
6 (&)	36	26	36	26
7 (')	37	27	37	27
8 (()	38	28	38	28
9 ())	39	29	39	29
: (*)	3A	2A	3A	2A
; (+)	3B	2B	3B	2B
@ ( )	40	60	40	60
[({)	5B	7B	4B	7B
\ (:)	5C	7C	5C	7C
] (})	5D	7D	5D	7D
^ (—)	5E	7E	5E	7E
A	61	41	01	01
B	62	42	02	02
C	63	43	03	03
D	64	44	04	04
E	65	45	05	05
F	66	46	06	06
G	67	47	07	07
H	68	48	08	08
I	69	49	09	09
J	6A	4A	0A	1A
K	6B	4B	0B	1B
L	6C	4C	0C	1C
M	6D	4D	0D	1D
N	6E	4E	0E	1E
O	6F	4F	0F	1F
P	70	50	10	00
Q	71	51	11	11
R	72	52	12	12
S	73	53	13	13
T	74	54	14	14
U	75	55	15	15
V	76	56	16	16
W	77	57	17	17
X	78	58	18	18
Y	79	59	19	19
Z	7A	5A	1A	1A
DEL (_)	7F	5F	7F	5F

control set Bit 6 and 7 and "0"

```
ENTER COMMANDS
>TE CRT (CR)
>RU (CR)
CRT    Version  n.n    mm/dd/yy    LOADED

PRESS THE RETURN KEY AFTER THE ' ' CHARACTER HAS BEEN PRINTED
IF ONE OF THE CHARACTERS IS NOT PRINTED ACCORDING TO THE SPECIFICATION, ASSUME
SOMETHING IS WRONG
!"#$%'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[/]'abcdefghijklmnopqrstu
vwxyz{¦}
(RETURN Key pressed by operator)
CRT SUBTEST 001 EXITED
Z000000000000000000000000000000000000000000000000000000000000000000000000000000000000Z
        .
        .
        .
Z000000000000000000000000000000000000000000000000000000000000000000000000000000000000Z
(RETURN Key pressed by operator)
CRT SUBTEST 002 EXITED
CRT SUBTEST 003 EXITED
PRESS ALL KEYS AND VERIFY WITH SPECIFICATION - EXIT BY "RETURN" KEY
(Echoed keyboard inputs, press RETURN to exit)
CRT SUBTEST 004 EXITED
ENTER  COMMANDS
>
```

Figure 8-4 Expected Results For Normal CRT Test Procedures

Example 1. Normal Testing

```
ENTER COMMANDS
>TE CRT (CR)
>SU NN (CR)
>RU (CR)
CRT    Version  n.n    mm/dd/yy    LOADED
   (subtest under testing)
CRT SUBTEST NN PASSED
ENTER COMMANDS
>
```

NOTE: 1. NN = valid subtest number
2. All subtests will print out exit message only

Example 2. Intermixing Commands Options

```
>TE CRT (CR)
>DE CENPTR (CR)          (select printer as output media)
>ME LPT (CR)             (error message only)
>RE 3 (CR)               (repeat 3 times)
>SU NN (CR)
>RU (CR)
   (test starts running)
.
.
.
ENTER COMMANDS           (this will be printed when subtest NN
>                        is repeated 3 times and finished)
```

8.1.3.5 PRINTER Test

This test provides the capability to diagnose the Centronics Printer subsystem through a series of subtests. A pass/fail message is printed when each subtest has finished. All subtests should be run in sequence to enhance the diagnostic capability.

Only the ASCII characters and controls valid for the Centronics Printer are tested. Valid characters and controls are listed in Table 8-11.

Normal Load Procedure. After the message "ENTER COMMANDS" a ">" should appear on the first column of the next line (Note: The ">" symbol indicates a key entry is required by the operator). The operator enters, via keyboard, the TEst command followed by a space, the filename of the Centronics Printer test (CENPTR) and a carriage return (CR). The operator then enters the RUn command to start the loading and executing. A self-explanatory example is given below.

Example:

```
ENTER COMMANDS
>TE CENPTR (CR)
>RU (CR)
>CENPTR    Version  n.n    mm/dd/yy    LOADED
```

Where underlined characters are entered by the operator, the digits after the filename are the version number and the release date for the CENPTR test program.

TABLE 8-11 VALID CHARACTERS AND CONTROLS FOR PRINTER TEST

CHARACTER	FUNCTION
07	bell
0A	line feed
0B	vertical tab
0C	form feed
0D	carriage return
0E	expanded characters
11	select
13	deselect
1B	escape code
20	space
21-7E	graphics
7F	delete

Load Error Procedure. If a load error occurs during the loading of the printer test program, the following messages will appear:

```
CENPTR  Version  n.n   mm/dd/yy   LOADED
  CHECKSUM ERROR (XXH) FOUND
  .
  .
  .
```

The test program has been loaded and started, but a checksum error was found, therefore, a reload should be attempted, possibly through a different diskette drive.

Normal Operating Procedures. All the required subtests - manual and automatic - will be run sequentially in a normal test procedure. Subtests that require operator intervention must be accomplished through operator interaction. They are described under the appropriate subtest. Table 8-12 lists the Printer Test subtests.

EXAMPLE:

```
ENTER COMMANDS
>TE CENPTR (CR)
>RU (CR)
CENPTR   Version  n.n   mm/dd/yy   LOADED
```

Any messages generated by the subtest occur here, manual routines usually need a keyboard response from the user in addition to the manual procedure requested.

EXAMPLE:

```
CENPTR subtest NN passed/exited

ENTER COMMANDS
>
```

Where: NN = Valid subtest number

Subtests which are self checking generate a "passed" completion message and the ones which should have the printer output visually checked generate an "exited" completion message. Figure 8-5 shows a display of expected results for normal operation of the printer test.

TABLE 8-12 DESCRIPTION OF PRINTER TEST SUBTESTS AND ERROR HANDLING

ATTRIBUTES AND FUNCTIONS
Subtest 1 (Required, Automatic) Status and SELECT test: Check the printer status bits for proper setting. Test the proper operation and timing of BUSY for both printing and non-printing characters (non-printable characters do not generate a BUSY signal). Verify that an interrupt occurs when BUSY signals that the printer operation is complete.
Subtest 2 (Required, Automatic) Printable ASCII Character Set Test: Print the entire printable ASCII character set. The printout should be checked visually for print quality, any missing dots, and that all 132 positions are printed.
Subtest 3 (Required, Automatic) Printable Elongated ASCII Character Set Test: Print the entire printable ASCII character set in elongated characters with half on one line and half on the next line. The printout should be checked visually for print quality, correct operation and any missing dots.
Subtest 4 (Required, Automatic) Print Single Elongated ASCII Character Set Test: Print the entire printable ASCII character set in 3 lines alternating between elongated and normal characters. The printout should be checked visually for correct operation.
Subtest 5 (Required, Automatic) Print Head Stepper Motor Test (Print Mixed number): Print the numerics 9,0,8,1,7,2,6,3,5,4 in order to produce the printout 0123456789 near the center of the page by printing in the forward and reverse direction without any line feeds. This is to test the print head stepper motor forward and reverse and the print character counter. The printout should be visually checked for print quality and no line feeds.
Subtest 6 (Required, Automatic) Audio Alarm Test: The audio alarm is activated under program control. A message is displayed on the CRT to alert the user to listen for it (applicable for model 702 printer only).
Subtest 7 (Required, Automatic) Delete Test: The message "DELETE TEST FAILED" is sent to the printer followed by the Delete control character and a Carriage Return control character. If the message is printed, the test failed. The printout should be visually checked for correct operation.
Subtest 8 (Required, Manual) Forms Feed Test: A forms feed is performed to position the forms at the top of a page, seven minus characters are printed followed by a second form feed which should put the form at the top of a new page. Seven more minus characters are printed. The printout should be checked for proper vertical page size (11 inches).

TABLE 8-12 (cont.)

Subtest 9 (Required, Manual) Manual Select and Deselect Test: The user is prompted to manually deselect the printer by pressing the SELECT switch; the deselected status is verified. The user is then prompted to press the SELECT switch to select the printer and the selected status is verified. When the user is prompted to enter R (CR) to continue, entering (CR) only will cause the subtest to terminate.
Subtest 10 (Required, Manual) Paper Out Test: The user is prompted to tear off the forms at the perforation just before entry into the printer. Repetitive line feeds (132 maximum) are performed until the paper runs out and the paper empty signal is detected.

```
ENTER COMMANDS
>TE CENPTR (CR)
>RU (CR)
CENPTR    Version  n.n    mm/dd/yy    LOADED

CENPTR SUBTEST 001 PASSED
CENPTR SUBTEST 002 EXITED
CENPTR SUBTEST 003 EXITED
CENPTR SUBTEST 004 EXITED
CENPTR SUBTEST 005 EXITED

LISTEN FOR AUDIO ALARM ON PRINTER

CENPTR SUBTEST 006 EXITED
CENPTR SUBTEST 007 EXITED
CENPTR SUBTEST 008 EXITED

(1)  PRESS PRINTER SELECT SWITCH (DESELECT PRINTER).
(2)  ENTER R (CR) FROM THE KEYBOARD WHEN READY.
(3)  PRESS PRINTER SELECT SWITCH (SELECT PRINTER).
(4)  ENTER R (CR) FROM THE KEYBOARD BWEN READY.
R
R
CENPTR SUBTEST 009 PASSED
(1)  TEAR PRINTER PAPER OFF AT ENTRY TO PRINTER.
(2)  ENTER R (CR) FROM THE KEYBOARD WHEN READY.

CENPTR SUBTEST 010 PASSED

ENTER  COMMANDS
>
```

Figure 8-5 Expected Results For Normal Operation Of Printer Test

Optional Operating Procedures. Refer to Table 8-3 for the diagnostic commands summary.

The command options can be intermixed. The following self-explanatory examples apply to all of the subtest unless otherwise specified:

Example 1. Normal Testing

```
ENTER COMMANDS
>TE CENPTR (CR)
>SU NN (CR)
>RU (CR)
CENPTR    Version  n.n    mm/dd/yy    LOADED
   (subtest under testing)
CENPTR SUBTEST NN PASSED
ENTER COMMANDS
>
```

NOTE: NN = valid subtest number

Example 2. End a Subtest Before Completion:

```
   .
   .
   .
   (Same as in Example 1)
   .
   .
   .
   (Test is running)
   (Press ESC Key)
CPU SUBTEST NN ENDED
ENTER COMMANDS
>
```

Example 3. Intermixing Commands Options

```
>TE CENPTR (CR)
>DE CRT (CR)                (select CRT as output media)
>ME ERROR (CR)              (error message only)
>RE 3 (CR)                  (repeat 3 times)
>SU NN (CR)
>RU (CR)
   (test starts running)
CENPTR    Version  n.n    mm/dd/yy    LOADED
   .
   .
   .
ENTER COMMANDS              (this will be printed when subtest NN
>                           is repeated 3 times and finished)
```

Error Recovery. When a subtest fails (status error, comparison error, etc.) an error message is printed. If an error is encountered which is considered recoverable, the subtest will print the pertinent information and continue. Unrecoverable errors will cause the subtest to return to the DM. The subtest can be restarted by entering the appropriate commands.

Error Message. The error message consists of device name, a subtest number, and an error number as follows:

```
CENPTR SUBTEST NN ERROR MM

Where NN = subtest number
      MM = error code
```

Refer to Table 8-13 for further details.

8.1.3.6 Diskette Drive Test

This test provides the capability to diagnose the diskette drive subsystem, which consists of the double density disk controller and dual diskette drive modules, through 13 different subtests. A pass/fail message is printed when each subtest has finished. All subtests should be run in sequence to enhance the diagnostic capability. Table 8-14 lists the subtests.

Subtest 1 is designed to check the ready status and write protect status. Subtest 2 is designed to check the disk controller on-board memory. Subtest 3 and 4 are designed to interrogate the communication channels (I/O) addresses and latches. Subtest 5 is designed to check the interrupt circuitry. Subtest 7 is designed to exercise the seek function. Subtests 6, 8 and 9 are designed to exercise on-board firmware and to test the read/write logic, disk conditions, and head alignment. Subtests 10, 11 and 12 are designed for hard failures in read/write logic or stepper motor. Subtest 13 is designed to allow the user to specify an IOBP for special testing.

Normal Loading Procedure. After the message "ENTER COMMANDS" a ">" should appear on the first column of the next line (Note: The ">" symbol indicates a key entry is required by the operator). The operator enters via keyboard, the TEst command followed by a space, the file name of the Diskette Drive test (FLOPPY) and a carriage return (CR). The operator then enters the RUn command to start the loading and executing. A self-explanatory example is given below:

Example:

```
ENTER COMMANDS
>TE FLOPPY (CR)
>SU ALL (CR)
>RU (CR)
FLOPPY    Version  n.n    mm/dd/yy    LOAD
.
.
.
```

Where underlined characters are entered by the operator, the digits after the filename are the version number and the release date for the floppy test program. Refer to Table 8-3 for keyboard input command format.

TABLE 8-13 PRINTER TEST ERROR TABLE

SUBTEST NUMBER	ERROR NUMBER	EXPLANATION	SUGGESTED ACTION	ACTION
Initialization Routine and all subtests	01	Printer Module incorrect; status bit 7 off	1,2,3,4,5	1. If printer is not a Centronics, discontinue test. 2. Verify printer main power on, restart test. 3. Check printer cable and replace if defective. 4. Replace System Processor Board. 5. Replace printer. 6. Put forms in printer and/or check switch operation, restart test. 7. If paper is not out, repeat the subtest following the directions.
	02	Video Circuit light not detected; status bit 2 off	1,2,3,4,5	
	04	No fault detected; status bit 3 off	1,2,3,4,5	
	05	Paper empty; status bit 4 off	6,1,2,3,4,5	
	06	Printer not selected; status bit 5 off	1,2,3,4,5	
	07	Fault detected; status bit 3 on	1,2,3,4,5	
	08	Busy on incorrectly; status bit 0 off	1,2,3,4,5	
	09	Busy not on; status bit 0 on	1,2,3,4,5	
	10	Busy not reset; status bit 0 off	1,2,3,4,5	
	11	No printer Interrupt	1,2,3,4,5	
	12	Paper not empty test failed	7,1,2,3,4,5	
	14	Unsolicited Interrupt	1,2,3,4,5	
7	'Delete Test Failed' message on Centronics		1,2,3,4,5	

TABLE 8-14 DISKETTE DRIVE TEST SUBTESTS

ATTRIBUTES AND FUNCTIONS
Subtest 1 (Required, Manual) Status check. Drives are continuously checked for ready status and write protect status. These conditions are read and displayed on the CRT screen or on the printer, if desired. Diskettes are inserted alternately into the drives A and B and the status is checked. The test is exited by pressing any key.
Subtest 2 (Required, Automatic) On-board memory test. The disk controller memory is tested with Hex 00, FF, AA, 55 data patterns. An addressing test is also performed. When errors are detected, the address, contents, and the expected contents are displayed.
Subtest 3 (Required, Automatic) Input/Output latch test. The command latches are forced to certain patterns, the status latches are polled and compared with expected result (i.e., IOPB is sent via 5555H, AAAAH, and FFFFH).
Subtest 4 (Required, Automatic) Input/Output address response. Commands are sent to and status read from correct addresses and address error groups are polled for proper response. Incorrect addresses are then used for commands (addresses above BASE are used). The error groups are polled for no change in status.
Subtest 5 (Required, Automatic) Interrupt test. The capability of the disk controller to interrupt the central processor is tested.
Subtest 6 (Required, Manual) Format test. Commands are issued to format a disk, then checks the disk for correct format through a read operation. This is repeated for both sequential and random track formats. A scratch diskette must be used for this test.
Subtest 7 (Required, Manual) Head position test. The disk controller is issued a RESTORE command, and the test checks for track 00 within 1 sec. A STEP-IN command is then issued and the test checks for track 01. Successive step commands are issued to track 76, verifying each track number as encountered. A STEP-OUT command is issued followed by successive step commands back to track 0. Several SEEK commands are issued and verified for different directions.
Subtest 8 (Required, Manual) Write test. A C7H data pattern is written on the entire scratch disk. Subtest 9 is used to read this data. The drive used must be selected.
Subtest 9 (Required, Manual) Read test. The data written in Subtest 8 is read and verified with a retry level of zero. This subtest may be used on the same drive that was used in Subtest 8 or a different drive.

TABLE 8-14 (cont.)

Subtest 10 (Utility Test) Continous Write. A continous series of write data commands are issued to write one track (physical track 77). This allows measurements to be taken to isolate a write malfunction. The operator can specify the data pattern; either all 0's or 1's (default is all 0's).
Subtest 11 (Utility Test) Continous Read. A continous series of read data commands are issued to read one track (physical track 77). This allows measurements to be taken to isolate a read malfunction.
Subtest 12 (Utility Test) Stepper motor. Alternating STEP-IN and STEP-OUT instructions are issued to the head stepper motor to allow measurements to be taken.
Subtest 13 (Utility Test) IOPB test. This subtest allows the operator to specify any valid parameter(s) for the IOPB structure, send the IOPB to the controller, and display the status when done.

Load Error Procedure. If a load error occurs during the loading of the diskette drive test program, the following messages will appear:

```
FLOPPY    Version  n.n    mm/dd/yy    LOADED
CHECKSUM ERROR (XXH) FOUND
.
.
.
```

The test program has been loaded and started, but a checksum error was found. Therefore, a reload should be attempted, possibly through a different diskette drive.

Normal Operating Procedures. All the required subtests - manual and automatic - will be run sequentially in a normal test procedure through the commands. There are from subtest 1 to subtest 9 (Subtests 10-13 are utilities and not required subtests). Drive 0 will be used as default when the operator fails to select the drive number. Subtests that require operator intervention must be accomplished through operator interaction. They are described below in detail:

An initialization routine will be invoked whenever a RUn command has been entered by the operator (see example under normal load precedures). The operator is also responsible for entering a valid drive number followed by a CR, which will be used by all the following subtests.

After the initialization message is printed, the operator must complete the following steps:

1. Remove the Diagnostic System diskette.

2. Do NOT load the formatted scratch diskette for required test run.

3. Enter the drive number which is to be tested (CR only will default to drive 0). Drive 0 is physically the left hand drive and is labeled 'A', and likewise drive 1 is physically the right hand drive and is labeled 'B' (as viewed from the front of the unit).

4. If the drives are single sided, the "sides >" question must be answered with zero. If double sided enter the side you wish to test. (CR only will default to single sided).

   Note: Double sided test not supported at this time.

5. The subtest 1 will start right after the last CR.

The purpose of subtest 1, status check, is to display/print all the status bits pertinent to all drives. A scratch diskette can be loaded and unloaded from any of the available drives. The write protect switch is tested by removing the tape which covers the write protect notch on the diskette.

The status will be shown on the output media in the following format:

```
DRIVE     0  1
RDY       X  X
WPT       Y  Y
```

Where RDY = disk ready
WPT = write protect
X = 1 if ready, 0 if not ready
Y = 1 is write protected, 0 if not write protected

To run subtest 1, complete the following steps:

1. After the initialization stage, check that the status is all zero (no diskette in drives).

2. Starting at drive 0, load the scratch diskette with write protect tape on. Compare the status on the output media with the expected status. Proceed to the next drive until all drives have been tested.

3. Remove the write protect tape, and repeat Step 2 using drive B.

4. Check both drives randomly.

5. Before exiting from this subtest, insert the scratch diskette into the 'to be tested drive' (selected in initialization stage), then press ANY key.

6. If the scratch diskette is not present, a message 'Mount diskette in drive n, press RETURN key' will appear for some subtests. Repeat step 5 to start the follow-on subtests.

NOTE: 1. Refer to the expected results, Figure 8-6 or (Table 8-15), for further explanation.
2. A scratch diskette must be used to avoid modification of the diskette (a Format command will be used to accomplish subtest 6).
3. Do NOT insert or pop the diskette when the drive has been selected (i.e., the LED of the drive is on). This will hang the system because of the Format command. In case the system hangs itself, inserting the diskette (or pop it) will release the system back to subtest 1 again.

If an error is detected while running the test program, the operator should refer to the error procedures.

Subtests 2 through 5 are automatically run.

```
ENTER COMMANDS
>TE FLOPPY (CR)
>SU ALL (CR)
>RU (CR)
FLOPPY    Version  n.n    mm/dd/yy    LOADED

1.  Remove diagnostic system floppy diskette                    Operator should
2.  Load a formatted scratch floppy diskette (if necessary)     only complete steps
3.  Enter the drive number to be tested                         1 and 3 at this time

Drive - 0,1,>M          where M is the number of the drive being tested.
Density - S or D>K      where K is the density of the scratch disk to be used.
Side - 0 or 1>N         where N is the side to be accessed.
                        (Must be 0 for single sided drives.)

DRIVE   0  1            (Before loading the scratch floppy diskette, status should
RDY     X  X            be all zeros.  Load the diskette into drive 0, X should
WPT     Y  Y            change from 0 to 1, Y should be 1 or 0 depends if the write
                        protect tape is absent or not.  Repeat this for other drive.)
                        Press any key
                        (Before pressing any key, the operator should load the scratch
                        floppy diskette into drive M).

FLOPPY SUBTEST 002 PASSED
FLOPPY SUBTEST 003 PASSED
FLOPPY SUBTEST 004 PASSED
FLOPPY SUBTEST 005 PASSED
FLOPPY SUBTEST 006 PASSED
FLOPPY SUBTEST 007 PASSED
FLOPPY SUBTEST 008 PASSED
FLOPPY SUBTEST 009 PASSED
ENTER  COMMANDS
>
```

NOTE: 1. Operator inputs are underlined.

2. Instructions to right of figure are not printed.

3. No pass/fail message for subtest 1.

4. In automatic test (i.e., SU AU) only subtest 2, 3, 4, and 5 will be tested.

Figure 8-6 Expected Results for Diskette Drive Test Normal Operation Procedures

Optional Operating Procedures. Refer to Table 8-3 for the diagnostic commands summary.

The command options can be intermixed. The following self-explanatory examples apply to all of the subtests unless otherwise specified:

Example 1. Normal Testing

```
ENTER COMMANDS
>TE FLOPPY (CR)
>SU NN (CR)
>RU (CR)
FLOPPY   Version  n.n    mm/dd/yy    LOADED
1.  Remove diagnostic system diskette
2.  Load a formatted scratch diskette (if necessary)
3.  Enter the drive number to be tested
Drive - 0,1,2,3>M
Density - S or D>D
Side - 0 or 1>

(The operator should perform 1, 2, 3, above in sequence before pressing CR key.
Otherwise a message as described in Step 6, running subtest 1, will be displayed.)

FLOPPY SUBTEST NN PASSED
ENTER COMMANDS
>
```

NOTE:
1. NN = valid subtest number
2. M = valid drive number
3. The following requirements must be met before the subtest can be executed:
   a. A scratch diskette for subtest 1 and 7.
   b. A formatted scratch diskette for all other subtest.
   c. Diskette should be loaded before entering drive number and CR key.

Example 2. End a Subtest Before Completion:

```
.
.
.
   (Same as in Example 1)
.
.
.
Drive >M (CR)
   (Test is running)
   (Press ESC Key)
FLOPPY SUBTEST NN ENDED
ENTER COMMANDS
>
```

Example 3. Intermixing Commands Options

```
ENTER COMMANDS
>TE FLOPPY (CR)
>DE CRT (CR)                (select CRT as output media)
>ME ERROR (CR)              (error message only)
>RE 3 (CR)                  (repeat 3 times)
>SU NN (CR)
>RU (CR)
   (test starts running)
FLOPPY    Version  n.n    mm/dd/yy    LOADED
.
.
.
ENTER COMMANDS              (this will be printed when subtest NN
>                           is repeated 3 times and finished)
```

Read/Write Logic, Diskette Conditions and Head Alignment. Use of subtest 6, 8, and 9, in combination, allows checking the read/write logic and diskette conditions. By switching the drives in these three subtests, the head alignment between drives is checked.

NOTE: Previous data on the diskette will be destroyed by subtest 7 and subtest 8.

Subtest 10, Continous Write, will do continous writes on one track (physical track 77) with a fixed pattern (selected by the operator) until the ESC key is pressed. It could be used when a hardware failure is suspected in the drive. While running this subtest, the operator can take measurements. This is a utility subtest.

To run subtest 10, complete the following steps:

1. Prepare a formatted diskette (Subtest 6).

2. Do necessary functions (if any).

3. Enter commands with subtest number 10.

4. Enter desired pattern, 00 or 11. (the default pattern is 00)

5. Do necessary functions (if any).

6. Press ESC key to return control to the DM.

NOTE: Previous data on track 77 will be destroyed by this subtest.

Subtest 11, Continous Read, is run the same as subtest 10 except read logic is activated instead of write. This is a utility subtest. Run subtest 10 to get the desired pattern written onto the diskette.

Subtest 12, Stepper Moter Test, requires a formatted scratch diskette. The stepper motor is activated to seek back and forth between two adjacent tracks until ESC key is pressed. Measurements can be taken for further diagnostics. This is a utility subtest. Steps are the same as in subtest 10.

Subtest 13, IOPB Test, requests all parameters from the operator. When all the parameters for an IOPB are satisfied, the IOPB is sent to the disk controller. At the end, 3 status bytes are displayed on the output media. Refer to Table 8-15 for IOPB structure. The default parameters will be used if only CR has been entered.

TABLE 8-15 I/O PARAMETER BLOCK (IOPB)

The start of any disk operation occurs when the system processor writes out to the disk controller, through I/O addresses BASE+1 and BASE+2, the starting address of the IOPB. The IOPB can be located anywhere in the Main Memory and consists of either six or twelve consecutive bytes of control information.

The relative positioning of the bytes within the IOPB are shown below and the specific bit functions are presented in the following paragraphs.

IOPB:

	7	6	5	4	3	2	1	0
BYTE 1	Disk NO.			INT. CONT.		L/S	DISK CMD	
2	NUMBER OF SECTORS							
3	TRACK NUMBER							
4	SECTOR NUMBER							
5	BUFFER ADDRESS LOW							
6	BUFFER ADDRESS HIGH							
7	SECTOR LENGTH							
8	DATA MARK			RETRY LEVEL		1	BUFFER START	
9	BTR			BLOCK TAG				
10			SIDE			SD	DD	CH
11	NEXT IOPB ADDRESS LOW							
12	NEXT IOPB ADDRESS HIGH							

NOTE: In the case of six bytes IOPB it will be assumed.

1. Sector length = 256 bytes
2. Data mark = FBH Normal data mark
3. Retry level = 3
4. No chaining
5. IBM format
6. Single density, single side

BYTE 1

Bit 7,6	Drive Select
00:	Drive 0
01:	Drive 1
10:	Drive 2
11:	Drive 3

Bit 5,4	Specifies when to interrupt the main processor
00:	Never
01:	Error only
10:	After each IOPB
11:	After the last IOPB or in case of an error

Bit 3 Specifies the length of the IOPB to be used by the controller firmware
0: Six byte IOPB
1: Twelve byte IOPB

Bit 2,1,0 Specify disk commands
0: Transfer from disk to main memory
1: Transfer from main memory to disk
2: Format track sequential
3: Format track random
4: Transfer from buffer to main memory
5: Transfer from main main memory to buffer
6: Run test routine
7: Unassigned

BUFFER: 1K RAM in the disk controller

Byte 8 bits 2,1,0 specify the number of bytes to be transferred in case of commands 4 and 5.

BYTE 2

Number of sectors to be read/written must be 1 or greater; 0 is illegal.

BYTE 3

Track Number

Standard/double side floppy range 0 to 76

BYTE 4

Starting sector number

Range depends on sector length: must be 1 or any legal number.

BYTE 5

Low external buffer address

BYTE 6

High external buffer address

These two bytes are the pointer to the buffer area in main memory.

1. Source of data to be transfered to disk.
2. Source of data to be stored on disk.
3. Source of random sector numbers stored in random format.
4. Source of data to be transfered to the buffer.
5. Source of data stored during a buffer to main memory transfer.

BYTE 7

Sector Length

In case of IBM format: 01H 128 bytes
02H 256 bytes
03H 512 bytes
Rest not allowed

TABLE 8-15 (Cont.)

BYTE 8

Bit 7,6 Specifies Data Mark
00: F8H Deleted data mark
01: FBH Normal data

Bit 5,4 Retry Level
00: No retry
01: One (times 4; total 4 retries)
10: Two (times 4; total 8 retries)
11: Three (times 4; total 12 retries)

Bit 3 Specifies type of format
1: Always IBM format

Bit 2,1,0 Specify number of bytes to be transfered in memory/buffer transfers.

The buffer is divided into eight blocks of 128 bytes:

0: Transfer eight blocks starting from block 0
1: Transfer seven blocks starting from block 1
2: Transfer six block starting from block 2
3: Transfer five blocks starting from block 3
4: Transfer four blocks starting from block 4
5: Transfer three blocks starting from block 5
6: Transfer two blocks starting from block 6
7: Transfer one blocks starting from block 7

BYTE 9

Bit 7 Specifies Block Tag reporting in the event of an ERROR
0: Block tag not to be reported
1: Block tag to be reported

Bit 6 Unassigned

Bit 5,4,3,2,1,0 Specify Block Tag

Block tag allows the system processor to associate an I/O complete interrupt request from the controller to a specified link in a chain of IOPB's in the event of an error.

BYTE 10

Bit 7,6 Unassigned

Bit 5 Specifies side selection for double sided floppy
1: Side 1 selected
0: Side 0 selected

Bit 4,3,2 Unassigned

Bit 1 Specifies double density/single density
0: Single density diskettes
1: Double density diskettes

Bit 0 Specifies chaining of IOPB's
0: Last IOPB
1: More IOPB's to follow

TABLE 8-15 (Cont.)

BYTE 11

This specifies the eight least significant bits of the 16 bit main memory address pointing to the beginning of the next IOPB in the chain.

BYTE 12

This specifies the eight most significant bits of the 16 bit main memory address pointing to the beginning of the next IOPB in the chain.

A self-explanatory example is given below.

```
ENTER COMMANDS
>TE FLOPPY (CR)
>SU 13 (CR)
>RU (CR)
FLOPPY    Version  n.n    mm/dd/yy    LOADED

Option>___          (Yes or No;  if 'N' has been entered, test starts without asking the following
                    queries.  See notes on next page)
Drive>___           (# in decimal;  0 to 3 expected)
L/S IOPB>___        (Long or Short form)
Command>___         (# in decimal;  0 to 6 expected)
                    0-READ, 1-WRITE, 2-FORMAT SEQUENTIAL, 3-FORMAT RANDOM, 4-X'FER DDFDC TO MEMORY,
                    5-X'FER MEMORY TO DDFDC, 6-RUN TEST)
No. of sectors>___  (# in decimal;  NO_OF_SECTOR x SECTOR_LENGTH not to exceed 32K bytes for read,
                    otherwise DM will be overwritten when memory wraps around)
Track no.>___       (# in decimal;  this is the start track #)
Sector no.>___      (# in decimal;  this is the start sector #)
Sector length>___   (# in decimal;  1 to 3 expected, 1-128 bytes, 2-256 bytes, 3-512 bytes)
Retry>___           (# in decimal;  0 to 3 times)
Side>___            (# in decimal;  0 to 1)
Density>___         (Single or Double density)

          (test starts running)

Base+0 = XXH        (See status code message)
Base+1 = YYH
Base+2 = ZZH
```

NOTE: 1. If 'Y' has been entered for 'Option', all queries from 'Drive' thru 'Density' will be asked. Otherwise the default parameters will be used.

2. The default values for IOPB are:

Disk no. (drive):	0
Int. control:	* always after last IOPB or in case of error
L/S:	Short form (6 bytes)
Disk cmd:	READ
No. of sectors:	15
Track no.:	0
Sector no.:	1
Buffer address:	* always 8000H for all commands.

Sector length:	256 bytes (02H)
Data mark:	* always 0FBH
Retry level:	3
Format:	* always IBM format
Block in buffer:	* always start at block 0
Block tag byte:	* always 00H
Side:	0
Density:	Single density
Chain:	* always last IOPB
Next IOPB address:	* always 0000H

3. Underlined characters are expected input from operator.

4. Test starts running right after the last query is satisfied. Status message will be outputted to the output media when IOPB is done.

5. This subtest requires 64K Byte RAM (Due to buffer address 8000H being used).

Error Recovery. If an error is encountered which is considered recoverable, the subtest will print the pertinent information and continue until an error message is printed. All other errors will cause the subtest to return to the DM. The subtest can be restarted by entering the appropriate commands.

Error Messages. When the subtest fails (status error, comparison error, etc.) an error message is printed. The error message consists of device name, a subtest number and an error number as follows:

```
FLOPPY SUBTEST NN ERROR MM
```

Where NN = subtest
MM = error code

Refer to Table 8-16 for further details.

TABLE 8-16 DISKETTE DRIVE TEST ERROR TABLE

SUBTEST NUMBER	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
Initialization	Error 20	Invalid drive number or side number	Re-enter valid drive no. or side number
1	Subtest not correct	The drive did not reflect the expected status	1. Switch to the other drive to see if it still happens. If it does not, the first drive is bad. 2. Replace the BLC-8222 board
2	HHHH: PP=EE ERROR 01	-Mismatched on constant patterns (00,FF,55,AA) HHHH = Hexadecimal memory address PP=00,FF,55, AA received (in Hex)	Replace the BLC-8222 board
	HHHH: PP=EE ERROR 02	-Address pattern error	
3	ERROR 03	-Status does not reflect the forced address patterns on command latches for IOPB	1. Check DIP switch S2 if set per Appendix B 2. Replace the BLC-8222 board
4	ERROR 04	-I/O acknowledge signal fail to respond within 1 ms from legal I/O address	1. Check DIP switch S2 set up per Appendix B 2. Replace the BLC-8222 board
	ERROR 05	-Illegal I/O address responded	
5	ERROR 06	-Constant interrupt -Interrupt too late -Interrupt lost	1. Check DIP switch S1 set up per Appendix B 2. Replace the BLC-8222 board
6	Track = TTD ERROR 09	-Sequential seek command failed (at track number shown) TT=Track no. used D =Density (D=Double or S= Single)	1. Unformatted floppy disk used 2. Replace the BLC-8222 3. Replace drive (if all disks failed) 4. Replace the BLC-8222 board
	Track = TTD ERROR 10	-Random seek command failed (not found)	
7	Track = TTD ERROR 11	-Sequential format failed to be formatted on track no. shown TT=Track no. used D =Density (D or S)	1. Replace bad disk 2. Replace drive (speed is off)
	ERROR 12	-Random format failed to be formatted on track number shown	3. Replace the BLC-8222 board

TABLE 8-16 (Cont.)

SUBTEST NUMBER	ERROR CONDITION	EXPLANATION	SUGGESTED ACTION
8	Track = TTD ERROR 13	-Write operation failed at track number(s) specified TT=Track no. used D =Density (D or S)	1. Unformatted floppy disk used 2. Replace bad disk 3. Replace drive (speed is off) 4. Replace the BLC-8222 board
9	Track = TTD ERROR 14 HHHH: PP=EE ERROR 15	-Read operation failed at track number(s) specified TT=Track no. used D =Density (D or S) -Read data and expected data mismatched at sector number specified HHHH=Hex address *Left-most 9 bits are sector no. (in Hex) for 128-byte sector format *Left-most-byte is the sector number in Hex for 256 byte sector format *Left-most 7 bits are sector no. in Hex for 512-byte sector format PP = data pattern expected EE = data pattern received	1. Unformatted disk used 2. Replace bad disk 3. Replace drive (speed is off) 4. Replace the BLC-8222 board
10	STATUS CODE ERROR 21	-Continous write stopped	See Status Message at end of table
11	STATUS CODE ERROR 21	-Continous read stopped	See Status Message
12	STATUS CODE ERROR 21	-Stepper motor stopped	See Status Message
13	Base+0 = XXH Base+1 = YYH Base+2 = ZZH	-See status code message for details. XX, YY, and ZZ are Hex numbers	
ALL	ERROR 22	-Unrecognized status returned	Replace the BLC-8222 board
ALL	ERROR 23	-Time out but still busy	1. Replace bad disk 2. Replace the BLC-8222 board
NOTE: Errors 16-19 are not used.			
OTHER MESSAGES: 1. 'Mount diskette in drive n, press RETURN key' - missing diskette in selected drive. 2. 'Retry has been performed on diskette' - 3 retries have been performed on the scratch floppy diskette.			

TABLE 8-16 (Cont.)

Status code message (at BASE+0):

'Status code = XXH'

Under normal conditions, the subtest when failed, should provide a status code message (equals to BASE+0 in sub. 13). The code is one byte and represented by two Hex digits. The explanations are given below:

Bits 7,6,5,4 - Error Group (first X)

F	=	Change in drive status
C,D	=	IOPB error
B	=	Seek, restore, stepping error
A	=	Read/write error
9	=	Write sector/format error

Bits 3,2,1,0 - Error Code (second X)

Error Group F:

Bit 3:1	Drive status 3 changed
Bit 2:1	Drive status 2 changed
Bit 1:1	Drive status 1 changed
Bit 0:1	Drive status 0 changed

Error Group C:

Bit 3:1	Disk command error
Bit 2:1	Sector number error
Bit 1:1	Track number error
Bit 0:1	Number of sectors error

Error Group D:

Bit 0:1	Sector length error

Error Group B:

Bit 2:1	Seek, step, restore CRC error; i.e., CRC error in ID field
Bit 1:1	Seek error
Bit 0:1	Drive not ready

Error Group A:

Bit 3:1	Lost data error; i.e., hardware timing error
Bit 2:1	Read/write CRC error; i.e., CRC error in data field
Bit 1:1	Record not found; i.e., the specific sector to read or to be written is missing

Error Group 9:

Bit 0:1	Write protect error in format or write sector

TABLE 8-16 (Cont.)

BASE+1

Bit 7 Specifies the state of DDFDC'S operation

1: The DDFDC is busy executing some given command
0: The last command specified by the IOPB has been executed

Bit 6 Error indicator

1: The command executed had an error
0: The command was executed successfully

Bit 5 Retry indicator

1: The command executed had a retry
0: The command executed without a retry

Bit 4 Unassigned

Bit 3,2,1,0 Specify state of drives 3,2,1,0 respectively

1: The respective drive is ready
0: The respective drive is not ready

BASE+2

Bit 7.6 Unassigned

Bit 5,4,3,2,1,0 Specify block tag of the last command executed with an error

STATUS at BASE+0,1 are always available, BASE+2 is made available when the system processor does a IN from this address port. It changes back to BASE+0 after the system processor has read the I/O address.

8.1.3.7 RS232C Serial Port Test

The purpose of the serial port test is to verify the operation of the unassigned RS232 Serial Port. The series of subtests listed in Table 8-17 are used.

Special Hardware Required

A special connector is required to run this test. A 25-pin E.I.A. connector (AMP #206604-2 78-22 or equivalent), with the pin connections below, must be plugged into the RS232 interface connector in the rear of the module. The test is meaningless without this special connector.

Connect pin #2 to pin #3
pin #4 to pin #5
pin #6 to pin #20

Normal Operating Procedure

All the required subtest (1-10) are run sequentially in a normal testing procedure. The example below shows the expected results during normal operating procedures.

Example:

```
ENTER COMMANDS
>TE SERIAL (CR)
>RU (CR)
SERIAL              Version n.n     mm/dd/yy          LOAD
PLACE CONNECTOR ON RS232 PORT AND HIT RETURN
SERIAL             SUBTEST 001       PASSED
SERIAL             SUBTEST 002       PASSED
SERIAL             SUBTEST 003       PASSED
SERIAL             SUBTEST 004       PASSED
SERIAL             SUBTEST 005       PASSED
SERIAL             SUBTEST 006       PASSED
SERIAL             SUBTEST 007       PASSED
SERIAL             SUBTEST 008       PASSED
SERIAL             SUBTEST 009       PASSED
SERIAL             SUBTEST 010       PASSED
ENTER COMMANDS
>
```

Error Message

Table 8-18 list all the errors for the Serial Port test.

TABLE 8-17 SERIAL PORT SUBTESTS

ATTRIBUTES AND FUNCTIONS
Subtest 1 (Required, Manual) 9600 Baud Subtest At 9600 Baud, this test transmits 50 characters through the serial port, then receives the same 50 characters through the serial port, verifying that the same characters are received. This process is repeated 12 times with different serial word formats (word lengths of 5, 6, 7 or 8 bits with 1, 1-1/2 or 2 stop bits.
Subtest 2 (Required, Manual) 4800 Baud Subtest Same as Subtest 1, at 4800 Baud.
Subtest 3 (Required, Manual) 2400 Baud Subtest Same as Subtest 1, at 2400 Baud.
Subtest 4 (Required, Manual) 1200 Baud Subtest Same as Subtest 1, at 1200 Baud.
Subtest 5 (Required, Manual) 600 Baud Subtest Same as Subtest 1, at 600 Baud.
Subtest 6 (Required, Manual) 300 Baud Subtest Same as Subtest 1, at 300 Baud.

TABLE 8-17 (Cont.)

ATTRIBUTES AND FUNCTIONS
Subtest 7 (Required, Manual) 150 Baud Subtest Same as Subtest 1, at 150 Baud.
Subtest 8 (Required, Manual) 110 Baud Subtest Same as Subtest 1, at 110 Baud.
Subtest 9 (Required, Manual) Interrupt Subtest Tests for the proper generation of an interrupt to the processor when the input buffer receives a complete character.
Subtest 10 (Required, Manual) Parity Subtest Parity is enabled and characters are transmitted and received with odd parity and even parity, alternating. Otherwise the same as Subtest 1.

TABLE 8-18 SERIAL PORT TEST ERROR TABLE

ERROR NUMBER	EXPLANATION	SUGGESTED ACTION
1	Parity error. Parity count of byte sent out is not the same as count of byte received.	Replace 8251 (or) Replace System Processor board
2	Overrun error. Data in the input buffer were not read by the processor before they were replaced by the next byte.	Replace System Processor board
3	Frame error. Stop bits framing the received byte were not correct.	Check connector Replace 8251 Replace System Processor board
4	Data mismatch error. Data received different from data sent.	Check connector Replace 8251 Replace System Processor board
5	No interrupt was received by the processor upon receipt of a complete character. This error can occur only in subtest 9.	Check for proper jumpers on System Processor board

NOTE: In all cases, if an error is detected, check the connector and rerun the tests before replacing or debugging board.

8.2 DISKETTE DRIVE MODULE MAINTENANCE

Maintenance of the diskette drive module may be required as a result of a failure, (indicated by the inability of the system to load software), by a diagnostic test result, or part of a periodic preventive maintenance procedure. Subsection 8.2.2 covers diagnostic tests of the diskette drive; Subsection 8.2.3 covers preventive maintenance procedures.

Before starting diagnostic procedures, complete the power supply checks in subsection 8.2.1.

This is a suggested maintenance program. To set up a different program refer to the appropriate Shugart or Siemans OEM manual listed bedow.

Shugart Associates Reference Manuals (For SA800)

- Maintenance manual SA800/801 Diskette Storage Drive
  Publications No. 50575-4 (2/78)

This manual is available from:

SHUGART ASSOCIATES
475 Oakmead Parkway
Sunnyvale, CA 94086
Telephone: (408) 733-0100
TWX: 910-339-9355 SHUGART SUVL

Siemans Corporation Reference Manuals (For FDD100-8)

- OEM Floppy Disk Drive FDD100-8 Technical Manual, Volume 1.
- OEM Floppy Disk Drive FDD100-8 Technical Manual, Volume 2.

These manuals are available from:

SIEMANS CORPORATION
OEM Division
240 E. Palais Road
Anaheim, CA 92805
Telephone: (714) 991-9700
Telex: 685691

8.2.1 Diskette Drive Module Power Supply Checks

Before starting power supply checks or diagnostic tests, the diskette drive module should be given a thorough visual inspection to ensure problems are not mechanical in nature. Checking that cable connectors are tight and rear-panel connectors are in place can eliminate many problems, especially those of an intermittent or random nature.

Voltage checks on the diskette drive power supply can be performed with any quality analog or digital multimeter having a minimum of 20 kOhms/volt sensitivity. Checks should be made at DC and AC power connectors of each drive. The connectors should be removed from both the drives to prevent erroneous readings due to loading effects. Figure 8-7 shows the pin arrangement of the J5/P5 DC power connector for both drives. Table 8-19 lists the expected DC voltage readings. Figure 8-8 shows the pin arrangement of the J4/P4 AC power connector for both drives. Table 8-20 lists the expected AC voltage readings. If the correct readings are obtained with the connectors removed, replace each connector in turn and recheck the voltage readings. This should indicate any loading problems due to an individual drive fault.

8.2.2 Diskette Drive Diagnostic Techniques

Incorrect operating procedures, faulty programming, damaged diskettes, soft errors (created by airborn contaminants), random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment.

Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

8.2.2.1 Soft Error Detection and Correction

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. Usually these contaminants can be removed by the cartridge self-cleaning wiper.

2. Random electrical noise that usually lasts for a few microseconds.

3. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.

4. Worn or defective load pad.

TABLE 8-19 DISKETTE DRIVE DC VOLTAGE READINGS

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (ptop)
1	+24VDC	±1.2VDC	1.7 A Max	100mv
2	+24V Return	---	---	---
3	-5V Return	---	---	---
4	-5VDC	±0.25VDC	0.07 A Max	50mv
5	+5VDC	±0.25VDC	1.0 A Max 0.8 A Typ	50mv
6	+5V Return	---	---	---

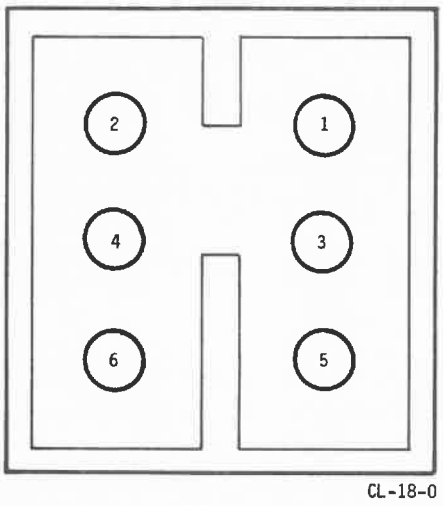


Figure 8-7 J5 Connector

TABLE 8-20 DISKETTE DRIVE AC VOLTAGE READINGS

P4 PIN	60 Hz		50 Hz	
	110/115V	208/230V	100V	230V
1	85-127 VAC	170-253 VAC	85-127 VAC	150-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127V Rtn	170-253V Rtn	85-127V Rtn	170-253V Rtn
MAX CURRENT	0.35 Amps	0.23 Amps	0.35 Amps	0.23 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

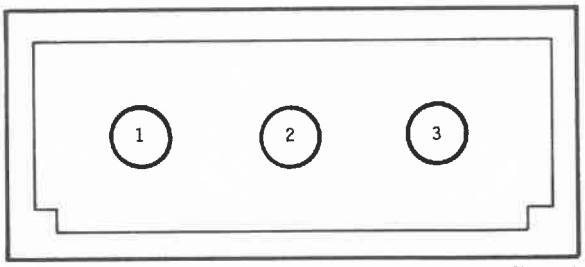


Figure 8-8 J4 Connector

The following procedures are recommended to recover from soft errors:

1. Reread the track twelve (12) times or until such time as the data is recovered.

2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat step 1.

4. If data is not recovered, the error is not recoverable.

8.2.2.2 Write Error

If an error occurs during a write operation, it could be detected on the next revolution by doing a read operation, commonly called a "write check". To correct the error, another write and write check operation must be done. If the write operation is not successful after twelve (12) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists the diskette should be replaced and the above precedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

8.2.2.3 Read Error

Most errors that occur will be soft errors. In these cases, performing an error recovery procedure will recover the data.

8.2.2.4 Seek Error

1. Stepper malfunction.

2. Improper carriage torque.

To recover from a seek error recalibrate to track 00 and perform another seek to the original track.

8.2.3 Preventive Maintenance

8.2.3.1 Introduction

The prime objective of any preventive maintenance (PM) activity is to provide maximum machine availability to the user. Every preventive maintenance operation should assist in realizing this objective.

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items during PM may save down-time later.

Remember, do not do more than recommended preventive maintenance on equipment that is operating satisfactorily.

8.2.3.2 Preventive Maintenance Procedures

The recommended maintenance operations are listed in Table 8-21. During normal preventive maintenance, perform only those operations listed on the chart for that preventive maintenance period. Details on adjustments and service checks can be found in the drive manufacturer's maintenance manual. Observe all safety procedures.

8.2.3.3 Cleanliness

Cleanliness cannot be overemphasized in maintaining the SA800. Do not lubricate the SA800; oil will allow dust and dirt to accumulate. The read/write head should be cleaned only when signs of oxide build up are present.

8.3 REPAIR AND RETURN

Any returns to the factory must be packed in either the original container or a substitute container of equal strength and durability. The original packing material or a substitute approximately 2 inches thick should surround all protruding surfaces, switches, etc. Each module must be packaged separately. Any loose equipment items that were shipped in a separate package for the returned unit should be packed and included with the return. A description of the equipment defect, the nature of its cause, and the name and address of the sender, should accompany each return shipment.

TABLE 8-21 RECOMMENDED DISKETTE DRIVE PREVENTIVE MAINTENANCE PROCEDURE

UNIT	FREQ MONTHS	CLEAN	OBSERVE
Read/Write Head	12	Clean Read/Write Head ONLY IF NECESSARY	Oxide build up
R/W Head Load Button	12*	Replace	
Stepper Motor and Lead Screw	12	Clean off all oil, dust, and dirt	Inspect for nicks and burrs
Belt	12	N/A	Frayed or weakened areas
Base	12	Clean base	Inspect for loose screws, connectors, and switches
Read/Write Head	12	N/A	Check for proper alignment

* Assuming normal usage.

Returned equipment is to be sent to the following address:

Microcomputer Service Center
675 Almanor Avenue
Sunnyvale, California 94086
Attn: Microcomputer Service Manager Ref: SRA#____
Mail Stop: 15236
Telephone: (408) 737-6270

Address correspondence to the following facility:

Domestic Contact:

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95051
Attn: Microcomputer Service Manager
Mail Stop: 15236
Telephone: (408) 737-6270

European Contact:

National Semiconductor GmbH
Industriestrasse #10
D8080 Fuerstenfeldbruck
West Germany
Telephone: (08141) 1371
Telex: 05-27649

In other countries, contact your local National Semiconductor Sales Office or Authorized Representative.

NOTE: Do not return any material to National Semiconductor without first obtaining a service return authorization number (SRA#). To obtain an SRA#, call the telephone number listed above.

Appendix G

SYSTEM LOADER PROGRAM LISTING

The following is an example of the small program at location 20H on the System disk:

```
          LXI     H,IOPB+1000H
          ORA     M                 ; INSERT DRIVE NO.
          MOV     M,A               ;   INTO IOPB
          MOV     A,L
          OUT     71H               ; SEND LOW BYTE OF IOPB
          MOV     A,H               ; READ DISK STATUS
          OUT     72H
CHKBSY:   IN      71H               ; READ DISK STATUS
          ANI     80H
          JNZ     CHKBSY            ; IF STILL BUSY, WAIT
          IN      71H
          ANI     40H
          JNZ     03FAH             ; IF DISK ERROR, BACK TO PROM
          MOV     A,M               ; OTHERWISE, SET DRIVE # IN [A]
          JMP     0FA00H            ; GO TO BOOT-LOADER
;
IOPB:     DB      0                 ; DRIVE # AND COMMAND
          DB      4                 ; # OF SECTORS TO BE READ
          DB      0                 ; STARTING TRACK
          DB      7                 ; STARTING SECTOR #
          DW      0F9EBH            ; RAM ADDRESS FOR FILE-HEADER
```

It is up to the user how the rest of the Track 0 Sector 1 (both in front of and after the small program) is to be configured. Refer to Figure 4-11 for the flow chart of the Boot Firmware.

NOTE: Location 03F3 Hex contains logic to clear the error flag and jump to the Boot Loader loading again. Users loader could jump to 03F3H when an operator error occurs.

Appendix H

SUMMARY OF OP CODES AND EXECUTION TIMES

This Appendix gives a summary of the Z80 instructions set. The instructions are logically arranged into groups as shown in Tables H-1. The table shows the assembly language mnemonic OP code, the actual OP code, the symbolic operation, the content of the flag register following the execution of each instruction, the number of bytes required for each instruction as well as the number of memory cycles and the total number of T states (external clock periods) required for the fetching and execution of each instruction.

TABLE H-1 SUMMARY OF Z80A OPCODES

DATA TRANSFER INSTRUCTION GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C Z P/V S N H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
LD r,r'	(r)<-(r')		01 r r'	1	1	4	r,r' Reg.
LD r,data	(r)<-data		00 r 110 data	2	2	7	000 B 001 C
LD r,(HL)	(r)<-((HL))		01 r 110	1	2	7	010 D
LD r,(IX+d)	(r)<-((IX)+d)		11 011 101 01 r 110 d	3	5	19	011 E 100 H 101 L
LD r,(IY+d)	(r)<-((IY)+d)		11 111 101 01 r 110 d	3	5	19	111 A
LD (HL),r	((HL))<-(r)		01 110 r	1	2	7	
LD (IX+d),r	((IX)+d)<-(r)		11 011 101 01 110 r d	3	5	19	
LD (IY+d),r	((IY)+d)<-(r)		11 111 101 01 110 r d	3	5	19	
LD (HL),data	((HL))<-data		00 110 110 data	2	3	10	
LD (IX+d),data	((IX)+d)<-data		11 011 101 00 110 110 d data	4	5	19	
LD (IY+d),data	((IY)+d)<-data		11 111 101 00 110 110 d data	4	5	19	
LD A,(BC)	(A)<-((BC))		00 001 010	1	2	7	
LD A,(DE)	(A)<-((DE))		00 011 010	1	2	7	
LD A,(addr)	(A)<-(addr)		00 111 010 addr L addr H	3	4	13	
LD (BC),A	((BC))<-(A)		00 000 010	1	2	7	
LD (DE),A	((DE))<-(A)		00 010 010	1	2	7	
LD (addr),A	(addr)<-(A)		00 110 010 addr L addr H	3	4	13	
LD A,I	(A)<-(I)	* IFF2 * 0 0	11 101 101 01 010 111	2	2	9	
LD A,R	(A)<-(R)	* IFF2 * 0 0	11 101 101 01 011 111	2	2	9	
LD I,A	(I)<-(A)		11 101 101 01 000 111	2	2	9	
LD R,A	(R)<-(A)		11 101 101 01 001 111	2	2	9	
LD rp,addr	(rp)<-addr		00 rp0 001 addr L addr H	3	3	10	rp Pair 00 BC 01 DE
LD IX,addr	(IX)<-addr		11 011 101 00 100 001 addr L addr H	4	4	14	10 HL 11 SP
LD IY,addr	(IY)<-addr		11 111 101 00 100 001 addr L addr H	4	4	14	
LD HL,(addr)	(H)<-(addr+1) (L)<-(addr)		00 101 010 addr L addr H	3	5	16	
LD rp,(addr)	(rp_H)<-(addr+1) (rp_L)<-(addr)		11 101 101 01 rp1 011 addr L addr H	4	6	20	
LD IX,(addr)	(IX_H)<-(addr+1) (IX_L)<-(addr)		11 011 101 00 101 010 addr L addr H	4	6	20	

DATA TRANSFER INSTRUCTION GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C Z P/V S N H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
LD IY,(addr)	(IY_H)<-(addr+1) (IY_L)<-(addr)		11 111 101 00 101 010 addr L addr H	4	6	20	
LD (addr),HL	(addr+1)<-(H) (addr)<-(L)		00 100 010 addr L addr H	3	5	16	
LD (addr),rp	(addr+1)<-(rp_H) (addr)<-(rp_L)		11 101 101 01 rp0 011 addr L addr H	4	6	20	
LD (addr),IX	(addr+1)<-(IX_H) (addr)<-(IX_L)		11 011 101 00 100 010 addr L addr H	4	6	20	
LD (addr),IY	(addr+1)<-(IY_H) (addr)<-(IY_L)		11 111 101 00 100 010 addr L addr H	4	6	20	
LD SP,HL	(SP)<-(HL)		11 111 001	1	1	6	
LD SP,IX	(SP)<-(IX)		11 011 101 11 111 001	2	2	10	
LD SP,IY	(SP)<-(IY)		11 111 101 11 111 001	2	2	10	
EX DE,HL	(DE)<->(HL)		11 101 011	1	1	4	
EX AF,AF'	(AF)<->(AF')		00 001 000	1	1	4	
EXX	(BC)<->(BC') (DE)<->(DE') (HL)<->(HL')		11 011 001	1	1	4	Register bank and auxiliary register bank exchange
EX (SP),HL	(H)<->(SP+1) (L)<->(SP)		11 100 011	1	5	19	
EX (SP),IX	(IX_H)<->(SP+1) (IX_L)<->(SP)		11 011 101 11 100 011	2	6	23	
EX (SP),IY	(IY_H)<->(SP+1) (IY_L)<->(SP)		11 111 101 11 100 011	2	6	23	
LDI	((DE))<-((HL)) (DE)<-(DE)+1 (HL)<-(HL)+1 (BC)<-(BC)-1	* 0 0	11 101 101 10 100 000	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)

LDIR	((DE))<-((HL))
	(DE)<-(DE)+1
	(HL)<-(HL)+1
	(BC)<-(BC)-1
	Stops if (BC)=0
	If (BC)≠0
	(PC)<-(PC)-2
	Repeats instr.
	until (BC)=0
		0 0 0	11 101 101
			10 110 000
				2
				2
					5
					4
						21
						16
							If (BC)≠0
							If (BC)=0
							(BC) set to 0 prior to LDIR causes instruction to loop thru 64K bytes.

LDD	((DE))<-((HL)) (DE)<-(DE)-1 (HL)<-(HL)-1 (BC)<-(BC)-1	① * 0 0	11 101 101 10 101 000	2	4	16	
LDDR	((DE))<-((HL)) (DE)<-(DE)-1 (HL)<-(HL)-1 (BC)<-(BC)-1 Stops if (BC)=0 If (BC)≠0, (PC)<-(PC)-2 Repeat instr. until (BC)=0	0 0 0	11 101 101 10 11 000	2 2	5 4	21 16	If (BC)≠0 If (BC)=0

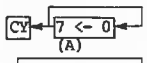
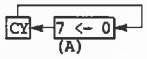
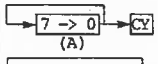
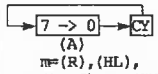
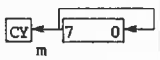
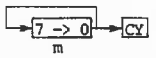
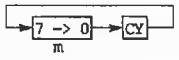
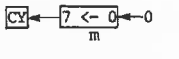
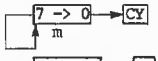
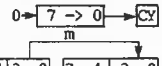
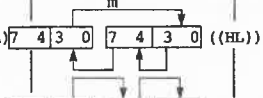
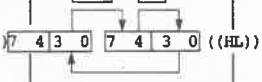
①: P/V flag is 0 if the result of BC-1=0, otherwise, P/V=1.

ARITHMETIC GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
ADD A,s	s=(r),data,(HL), (IX+d) or (IY+d)											
ADD A,r	(A)<-(A)+(r)	*	*	V	*	0	*	10 (000) r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A,data	(A)<-(A)+data	*	*	V	*	0	*	11 (000) 110 data	2	2	7	
ADD A,(HL)	(A)<-(A)+((HL))	*	*	V	*	0	*	10 (000) 110	1	2	7	
ADD A,(IX+d)	(A)<-(A)+((IX)+d)	*	*	V	*	0	*	11 011 101 10 (000) 110 d	3	5	19	
ADD A,(IY+d)	(A)<-(A)+((IY)+d)	*	*	V	*	0	*	11 111 101 10 (000) 110 d	3	5	19	
ADC A,s	(A)<-(A)+s+CY	*	*	V	*	0	*	001				See "ADD A,s" instructions for appropriate opcode bits, in cycles, T states and no. of bytes. Bits 543 shown here substitute for "ADD" bits in parenthesis.
SUB s	(A)<-(A)-s	*	*	V	*	1	*	010				
SBC A,s	(A)<-(A)-s-CY	*	*	V	*	1	*	011				
INC r	(r)<-(r)+1		*	V	*	0	*	00 r (100)	1	1	4	
INC (HL)	((HL))<-((HL))+1		*	V	*	0	*	00 110 (100)	1	3	11	
INC (IX+d)	((IX)+d)<-((IX)+d)+1		*	V	*	0	*	11 011 101 00 110 (100) d	3	6	23	
INC (IY+d)	((IY)+d)<-((IY+d)+1		*	V	*	0	*	11 111 101 11 110 100	3	6	23	
DEC m	m<-m-1		*	V	*	1	*	101				Bits 210 substitute for corresponding bits in INC r instructions.
DAA	Converts acc content into packed BCD following add or subtract with packed BCD operands	*	*	P	*		*	00 100 111	1	1	4	Decimal adjust accumulator.
CPL	(A)<-$\overline{(A)}$					1	1	00 101 111	1	1	4	Complement accumulator (one's complement)
NEG	(A)<-0-(A)	*	*	V	*	1	*	11 101 101 01 000 100	2	2	8	Negate acc. (two's complement)
CCF	CY<-$\overline{CY}$	*				0	X	00 111 111	1	1	4	Complement carry flag
SCF	CY<-1	①				0	0	00 110 111	1	1	4	Set carry flag
ADD HL, rp	(HL)<-(HL)+(rp)	*			0	0	X	00 rp1 001	1	3	11	rp Reg. 00 BC 01 DE 10 HL 11 SP
ADC HL, rp	(HL)<-(HL)+(rp)+CY	*	*	V	*	0	X	11 101 101 01 rp1 010	2	4	15	
SBC HL, rp	(HL)<-(HL)-(rp)-CY	*	*	V	*	1	X	11 101 101 01 rp0 010	2	4	15	
ADD IX,pp	(IX)<-(IX)+(pp)	*				0	X	11 011 101 00 pp1 001	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY,rr	(IY)<-(IY)+(rr)	*				0	X	11 111 101 00 rr1 001	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC rp	(rp)<-(rp)+1							00 rp0 011	1	1	6	
INC IX	(IX)<-(IX)+1							11 011 101 00 100 011	2	2	10	
INC IY	(IY)<-(IY)+1							11 111 101 00 100 011	2	2	10	
DEC rp	(rp)<-(rp)-1							00 rp1 011	1	1	6	
DEC IX	(IX)<-(IX)-1							11 011 101 00 101 011	2	2	10	
DEC IY	(IY)<-(IY)-1							11 111 101 00 101 011	2	2	10	

①: P/V flag is 0 if the result of BC-1=0, otherwise, P/V=1.

LOGICAL GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
RLCA		*				0	0	00 000 111	1	1	4	Rotate left circular accumulator
RLA		*				0	0	00 010 111	1	1	4	Rotate left accumulator
RRCA		*				0	0	00 001 111	1	1	4	Rotate right circular accumulator
RRA		*				0	0	00 011 111	1	1	4	Rotate right accumulator
RLC m	m=(R),(HL), (IX+d) or (IY+d)											Rotate left circular register r
RLC r		*	*	P	*	0	0	11 001 011 00 (000) r	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (HL)		*	*	P	*	0	0	11 001 011 00 (000) 110	2	4	15	
RLC (IX+d)		*	*	P	*	0	0	11 011 101 11 001 011 d 00 (000) 110	4	6	23	
RLC (IY+d)		*	*	P	*	0	0	11 111 101 11 001 011 d 00 (000) 110	4	6	23	
RL m		*	*	P	*	0	0	010				Instruction format and states are as shown for RLC m. To form new Op-code replace 000 of RLC,m with bits 543 shown. Flags, m cycles and T states correspond with RLC, m instructions.
RRC m		*	*	P	*	0	0	001				
RR m		*	*	P	*	0	0	011				
SLA m		*	*	P	*	0	0	100				
SRA m		*	*	P	*	0	0	101				
SRL m		*	*	P	*	0	0	111				
RLD		*		P	*	0	0	11 101 101 01 101 111	2	5	18	Rotate digit left and right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffected
RRD		*		P	*	0	0	11 101 101 01 100 111	2	5	18	

BIT MANIPULATION GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C	Z	P/V	S	N	H	OP-CODE 76	543	210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
BIT b,r	$Z \leftarrow -(r)_b$		*	X	X	0	1	11	001	011	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
								01	b	r				
BIT b,(HL)	$Z \leftarrow -((\overline{HL}))_b$		*	X	X	0	1	11	001	011	2	3	12	
								01	b	110				
BIT b,(IX+d)	$Z \leftarrow -((\overline{IX)+d})_b$		*	X	X	0	1	11	011	101	4	5	20	
								11	001	011				
									d					
								01	b	110				
BIT b,(IY+d)	$Z \leftarrow -((IY)+d)_b$		*	X	X	0	1	11	111	101	4	5	20	Bit b Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
								11	001	011				
									d					
								01	b	110				
SET b,m	m=(r),(HL), (IX+d) or (IY+d)													
SET b,r	$(r)_b \leftarrow 1$							11	001	011	2	4	8	
								11	b	r				
SET b,(HL)	$((HL))_b \leftarrow 1$							11	001	011	2	4	15	
								11	b	110				
SET b,(IX+d)	$((IX)+d)_b \leftarrow 1$							11	011	101	4	6	23	
								11	001	011				
									d					
								11	b	110				
SET b,(IY+d)	$((IY)+d)_b \leftarrow 1$							11	111	101	4	6	23	
								11	001	011				
									d					
								11	b	110				
RES b,m	$m_b \leftarrow 0$ m=(r), ((HL)), ((IX)+d) or ((IY)+d)							10						To form new OP-code replace bits 76 of last byte of SET b,m with 10. Flags and time states correspond to SET instruction.

LOGICAL GROUP

AND s	(A)←(A) s	*	*	V	*	1	X		100					Bits 543 replace the "000" in the ADD A,s instructions above.
OR s	(A)←(A) s	0	*	P	*	0	0		110					
XOR s	(A)←(A) s	0	*	P	*	0	0		101					
CP s	(A)-s	*	*	V	*	1	*		111					
CPI	(A)-((HL)) (HL)←(HL)+1 (BC)←(BC)-1		*	*	*	1	*	11	101	101	2	4	16	
								10	100	001				
			②	①										
CPIR	(A)-((HL))		*	*	*	1	*	11	101	101	2	5	21	If (BC)≠0 and (A)≠(HL)
	(HL)←(HL)+1							10	110	001	2	4	16	If (BC)=0 or (A)=(HL)
	(BC)←(BC)-1 Stop if (A)=(HL) or (BC)=0 otherwise (PC)←(PC)-2 Repeat instr. until (A)=((HL)) or (BC)=0													
			②	①										
CPD	(A)-((HL)) (HL)←(HL)-1 (BC)←(BC)-1		*	*	*	1	*	11	101	101	2	4	16	
								10	101	001				
			②	①										
CPDR	(A)-((HL)) (HL)←(HL-1) (BC)←(BC-1) Stop if (A)=(HL) or (BC)=0 otherwise (PC)←(PC)-2 Repeat until (A) = ((HL)) or (BC) = 0		*	*	*	1	*	11	101	101	2	5	21	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
								10	111	001	2	4	16	

① : P/V flag is 0 if the result of BC-1=0, otherwise, P/V=1

② : Z flag is 1 if A=(HL), otherwise Z=0

BRANCH GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C Z P/V S N H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
JP addr	(PC)<-(addr)		11 000 011 $addr_H$ $addr_L$	3	3	10	
JP cc,addr	If condition cc is true (PC)<-(addr) otherwise continue		11 cc 010 $addr_H$ $addr_L$	3	3	10	cc Condition 000 NZ non zero 001 Z zero 010 NC non carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign pos. 111 M sign neg.
JR e	(PC)<-(PC)+e		00 011 000 e-2	2	3	12	
JR C,e	If C=0, continue		00 111 000 e-2	2	2	7	If condition not met
	If C=1, (PC)<-(PC)+e			2	3	12	If condition is met
JR NC,e	If C=1, continue		00 110 000 e-2	2	2	7	If condition not met
	If C=0, (PC)<-(PC)+e			2	3	12	If condition is met
JR Z,e	If Z=0 continue		00 101 000 e-2	2	2	7	If condition not met
	If Z=1, (PC)<-(PC)+e			2	3	12	If condition is met
JR NZ,e	If Z=1, continue		00 100 000 e-2	2	2	7	If condition not met
	If Z=0, (PC)<-(PC)+e			2	3	12	If condition met
JP (HL)	(PC)<-(HL)		11 101 001	1	1	4	
JP (IX)	(PC)<-(IX)		11 011 101 11 101 001	2	2	8	
JP (IY)	(PC)<-(IY)		11 111 101 11 101 001	2	2	8	
DJNZ,e	(B)<-(B)-1 If (B)=0, continue		00 010 000 e-2	2	2	8	If B=0
	If (B)≠0, (PC)<-(PC)+e			2	3	13	If B≠0
CALL addr	$((SP)-1)<-(PC_H)$ $((SP)-2)<-(PC_L)$ (PC)<-(addr)		11 001 101 $addr_H$ $addr_L$	3	5	17	
CALL cc,addr	If condition cc is false continue normal program, else same as CALL addr		11 cc 100 $addr_H$ $addr_L$	3	3	10	If cc is false
				3	5	17	If cc is true
RET	$(PC_L)<-((SP))$ $(PC_H)<-((SP)+1)$		11 001 001	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET		11 cc 000	1	1	5	If cc is false
				1	3	11	If cc is true cc Condition 000 NZ non zero 001 Z zero 010 NC non carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign pos. 111 M sign neg.
RETI	Return from interrupt		11 101 101 01 001 101	2	4	14	
RETN	Return from non maskable interrupt		11 101 101 01 000 101	2	4	14	
RST p	$((SP)-1)<-(PC_H)$ $((SP)-2)<-(PC_L)$ $(PC_H)<-0$ $(PC_L)<-P$		11 t 111	1	3	11	t P 000 00H 001 08H 010 10H 011 18H 100 20H 101 28H 110 30H 111 38H

STACK, I/O, AND MACHINE GROUP

MNEMONIC	SYMBOLIC OPERATION	FLAGS C Z P/V S N H	OP-CODE 76 543 210	NO. OF BYTES	NO. OF M CYCLES	NO. OF T STATES	COMMENTS
IN A,(port)	(A)<-(port data)		11 011 011 port data	2	3	11	port to $A_0...A_7$ (A) to $A_8...A_{15}$
IN r,(C)	(r)<-((C))	* P * 0	11 101 101 01 r 000	2	3	12	C to $A_0...A_7$ B to $A_8...A_{15}$
INI	((HL))<-(port(C)) (B)<-(B)-1 (HL)<-(HL)+1	* ① X X 1 X	11 101 101 10 100 010	2	4	16	C to $A_0...A_7$ B to $A_8...A_{15}$
INIR	((HL))<-((C)) (B)<-(B)-1 (HL)<-(HL)+1 Stop if (B)=0 If (B)≠0, (PC)<-(PC)-2 Repeat until (B)=0	1 X X X 1 X	11 101 101 10 110 010	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0...A_7$ B to $A_8...A_{15}$
IND	((HL))<-((C)) (B)<-(B)-1 (HL)<-(HL)-1	* ① X X 1 X	11 101 101 10 101 010	2 2	4	16	C to $A_0...A_7$ B to $A_8...A_{15}$
INDR	((HL))<-(port(C)) (B)<-(B)-1 (HL)<-(HL)-1 Stop if (B)=0 If (B)-1≠0 (PC)<-(PC)-2	1 X X X 1 X	11 101 101 10 111 010	2 2	4 (If B=0) 5 (If B≠0)	16 21	
OUT (data)	(port data)<-(A)		11 010 011 port data	2	3	11	port data to $A_0...A_7$ (A) to $A_8...A_{15}$
OUT (C),r	(port(C))<-(r)		11 101 101 01 r 001	2	3	12	C to $A_0...A_7$ B to $A_8...A_{15}$
OUTI	(port(C))<-((HL)) (B)<-(B)-1 (HL)<-(HL)+1	* ① X X 1 X	11 101 101 10 100 011	2	4	16	C to $A_0...A_7$ B to $A_8...A_{15}$
OTIR	(port(C))<-((HL)) (B)<-(B)-1 (HL)<-(HL)+1 Stop if (B)=0 If (B)≠0, (PC)<-(PC)-2 Repeat until (B)=0	1 X X X 1 X	11 101 101 10 110 011	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0...A_7$ B to $A_8...A_{15}$
OUTD	((C))<-((HL)) (B)<-(B)-1 (HL)<-(HL)-1	① * X X 1 X	11 101 101 10 101 011	2	4	16	C to $A_0...A_7$ B to $A_8...A_{15}$
OTDR	((C))<-((HL)) (B)<-(B)-1 (HL)<-(HL)-1 Stop if (B)=0 If (B)≠0 (PC)<-(PC)-2 Repeat until (B)=0	1 X X X 1 X	11 101 101 10 111 011	2 2	5 (If B≠0) 4 (If B=0)	21 16	C to $A_0...A_7$ B to $A_8...A_{15}$
PUSH qq	((SP)-2)<-qq_L ((SP)-1)<-qq_H		11 qq0 101	1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	((SP)-2)<-IX_L ((SP)-1)<-IX_H		11 011 101 11 100 101	2	4	15	
PUSH IY	((SP)-2)<-IY_L ((SP)-1)<-IY_H		11 111 101 11 100 101	2	4	15	
POP qq	(qq_H)<-((SP)+1) (qq_L)<-((SP))		11 qq0 001	1	3	10	
POP IX	(IX_H)<-((SP)+1) (IX_L)<-((SP))		11 011 101 11 100 001	2	4	14	
POP IY	(IY_H)<-((SP)+1) (IY_L)<-((SP))		11 111 101 11 100 001	2	4	14	
NOP	No operation		00 000 000	1	1	4	
HALT	CPU halted		01 110 110	1	1	4	
DI	IFF<-0		11 110 011	1	1	4	
EI	IFF<-1		11 111 011	1	1	4	
IM 0	Set interrupt mode 0		11 101 101 01 000 110	2	2	8	
IM 1	Set interrupt mode 1		11 101 101 01 010 110	2	2	8	
IM 2	Set interrupt mode 2		11 101 101 01 011 110	2	2	8	

① : P/V flag is 0 if the result of BC-1=0, otherwise, P/V=1

Appendix I

Z80 CPU PIN DESCRIPTION

The Z80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in Figure I-1 and the function of each is described below.

A0-A15 (Address Bus)	Tri-state output, active high. A0-A15 constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.
D0-D7 (Data Bus)	Tri-state input/output, active high. D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
M1 (Machine Cycle one)	Output, active low. M1 indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, M1 is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. M1 also occurs with IORQ to indicate an interrupt acknowledge cycle.
MREQ (Memory Request)	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
IORQ (Input/Output Request)	Tri-state output, active low. The IORQ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An IORQ signal is also generated with an M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M_1 time while I/O operations never occur during M_1 time.
RD (Memory Read)	Tri-state output, active low. RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
WR (Memory Write)	Tri-state output, active low. WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
RFSH (Refresh)	Output, active low. RFSH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.

HALT
(Halt State)

Output, active low. HALT indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

WAIT
(Wait)

Input, active low. WAIT indicates to the Z80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

INT
(Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (IORQ during M1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

NMI
(Non Maskable Interrupt)

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than INT and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the Z80 CPU to restart to location 0066 Hex. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a BUSRQ will override a NMI.

RESET

Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

1. Disable the interrupt enable flip-flop
2. Set Register I = 00H
3. Set Register R = 00H
4. Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.

BUSRQ
(Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated.

BUSAK (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.
	Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

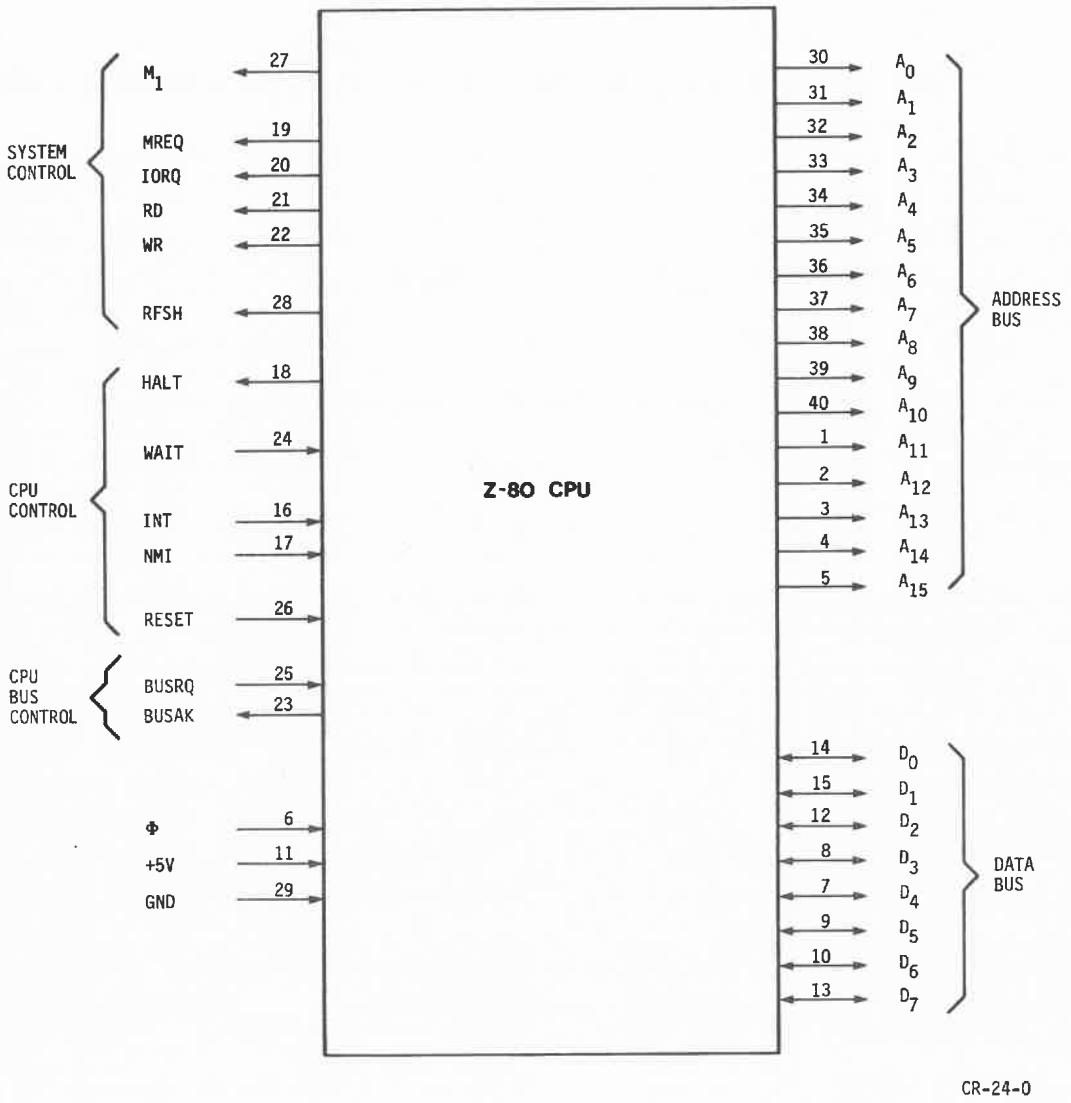


Figure I-1 Z80A Pin Configuration

Appendix J

BLC BOARD PIN ASSIGNMENTS, JUMPER CONFIGURATIONS AND ASSEMBLY DRAWINGS

This Appendix contains the pin assignments for each edge connector, for the three BLC boards in the base module.

- System Processor
- BLC-064 RAM
- BLC-8222 Disk Controller

The P1 pin assignments for all three boards are the same, thus they are shown only once in table J-1.

TABLE J-1 CONNECTOR P1 PIN ASSIGNMENTS COMMON TO ALL BOARDS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	+5V	4	+5V
5	+5V	6	+5V
7	+12V	8	+12V
9	-5V	10	-5V
11	GND	12	GND
13		14	INIT/
15	BPRN/	16	BPRO/
17		18	
19	MRDC/	20	MWTC/
21		22	IOWC/
23	XACK/	24	
25		26	
27	BHEN/	28	AD10/
29		30	AD11/
31		32	AD12/
33		34	AD13/
35	INT6/	36	INT7/
37	INT4/	38	INT5/
39	INT2/	40	INT3/
41	INT0/	42	INT1/
43	ADRE/	44	ADRF/
45	ADRC/	46	ADRD/
47	ADRA/	48	ADRB/
49	ADR8/	50	ADR9/
51	ADR6/	52	ADR7/
53	ADR4/	54	ADR5/
55	ADR2/	56	ADR3/
57	ADR0/	58	ADR1/
59	DATE/	60	DATF/
61	DATC/	62	DATD/
63	DATA/	64	DATB/
65	DAT8/	66	DAT9/
67	DAT6/	68	DAT7/
69	DAT4/	70	DAT5/
71	DAT2/	72	DAT3/
73	DAT0/	74	DAT1/
75	GND	76	GND
77		78	
79	-12V	80	-12V
81	+5V	82	+5V
83	+5V	84	+5V
85	GND	86	GND

TABLE J-2 SYSTEM PROCESSOR CONNECTOR P2 PIN ASSIGNMENTS

COMPONENT SIDE			SOLDER SIDE		
PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
1	BATT GND	Battery Ground	2	BATT GND	Battery Ground
3			4		8253 CS/
5			6		#1 8255 CS/
7			8		#2 8255 CS/
9			10		I/O Bus Request
11			12		#1 8251 CS/
13			14		#2 8251 CS/
15			16		#1 8259 CS/
17	PFS/	Power Fail Status	18		#2 8259 CS/
19	PFI/	Power Fail Interrupt	20		Override CS/
21			22		Memory Map CS/
23			24		
25			26		
27	M1/	Fetch Indicator	28	HLT/	Halt Indicator
29			30		
31			32		
33			34	BTMO/	Bus Time Out
35			36	INTA/	Interrupt Acknowledge
37			38	AUX RESET/	System Reset Switch Input
39			40	BPRN/	Bus Priority In
41			42		
43			44		
45			46		
47			48		
49			50		
51			52		
53			54		
55			56		
57			58		
59			60		

TABLE J-3 SYSTEM PROCESSOR CONNECTOR J1 PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND		
2	GND	2	Port E5 - Bit 7
3	GND	4	Port E5 - Bit 6
5	GND	6	Port E5 - Bit 5
7	GND	8	Port E5 - Bit 4
9	GND	10	Port E5 - Bit 3
11	GND	12	Port E5 - Bit 2
13	GND	14	Port E5 - Bit 1
15	GND	16	Port E5 - Bit 0
17	GND	18	Port E6 - Bit 3
19	GND	20	Port E6 - Bit 2
21	GND	22	Port E6 - Bit 1
23	GND	24	Port E6 - Bit 0
25	GND	26	Port E6 - Bit 4
27	GND	28	Port E6 - Bit 5
29	GND	30	Port E6 - Bit 6
31	GND	32	Port E6 - Bit 7
33	GND	34	Port E4 - Bit 7
35	GND	36	Port E4 - Bit 6
37	GND	38	Port E4 - Bit 5
39	GND	40	Port E4 - Bit 4
41	GND	42	Port E4 - Bit 3
43	GND	44	Port E4 - Bit 2
45	GND	46	Port E4 - Bit 1
47	GND	48	Port E4 - Bit 0
49	GND	50	

TABLE J-4 SYSTEM PROCESSOR CONNECTOR J2 PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	Port E9 - Bit 7
3	GND	4	Port E9 - Bit 6
5	GND	6	Port E9 - Bit 5
7	GND	8	Port E9 - Bit 4
9	GND	10	Port E9 - Bit 3
11	GND	12	Port E9 - Bit 2
13	GND	14	Port E9 - Bit 1
15	GND	16	Port E9 - Bit 0
17	GND	18	Port EA - Bit 3
19	GND	20	Port EA - Bit 2
21	GND	22	Port EA - Bit 1
23	GND	24	Port EA - Bit 0
25	GND	26	Port EA - Bit 4
27	GND	28	Port EA - Bit 5
29	GND	30	Port EA - Bit 6
31	GND	32	Port EA - Bit 7
33	GND	34	Port E8 - Bit 7
35	GND	36	Port E8 - Bit 6
37	GND	38	Port E8 - Bit 5
39	GND	40	Port E8 - Bit 4
41	GND	42	Port E8 - Bit 3
43	GND	44	Port E8 - Bit 2
45	GND	46	Port E8 - Bit 1
47	GND	48	Port E8 - Bit 0
49	GND	50	

TABLE J-5 SYSTEM PROCESSOR CONNECTOR J3 PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	MNEMONIC	PIN	MNEMONIC
1	#1 SEC TX DATA	2	
3	#1 TRANS SIG ELE TIMING	4	#1 TX DATA
5	#1 SEC RX DATA	6	#1 RX DATA
7	#1 REC SIG ELE TIMING	8	#1 RTS
9		10	#1 DTS
11	#1 SEC REQUEST TO SEND	12	#1 DSR
13	#1 DTR	14	SIG GND
15		16	#1 REC LINE SIG DET
17	#1 RING INDICATOR	18	
19	-12V (TTY ADAPTER POWER)	20	
21	#1 TRANS SIG ELE TIMING	22	+12V (TTY ADAPTER POWER)
23	+5V (TTY ADAPTER POWER)	24	
25	SIGNAL GND	26	#1 SEC CTS

TABLE J-6 SYSTEM PROCESSOR CONNECTOR J4 PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	MNEMONIC	PIN	MNEMONIC
1	#2 SEC TX DATA	2	
3	#2 TRANS SIG ELE TIMING	4	#2 TX DATA
5	#2 SEC RX DATA	6	#2 RX DATA
7	#2 REC SIG ELE TIMING	8	#2 RTS
9		10	#2 DTS
11	#2 SEC REQUEST TO SEND	12	#2 DSR
13	#2 DTR	14	SIG GND
15		16	#2 REC LINE SIG DET
17	#2 RING INDICATOR	18	
19	-12V (TTY ADAPTER POWER)	20	
21	#2 TRANS SIG ELE TIMING	22	+12V (TTY ADAPTER POWER)
23	+5V (TTY ADAPTER POWER)	24	
25	SIGNAL GND	26	#2 SEC CTS

TABLE J-7 BLC-064 RAM CONNECTOR P2 PIN ASSIGNMENTS

COMPONENT SIDE			SOLDER SIDE		
PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
1	GND	Signal Ground	2	GND	Signal Ground
3	*VCC AUX	+5 VDC Auxiliary	4	*VCC AUX	+5 VDC Auxiliary
5			6		
7	*VBB AUX	-5 VDC Auxiliary	8	*VBB AUX	-5 VDC Auxiliary
9			10		
11	*VDD AUX	+12 VDC Auxiliary	12	*VDD AUX	+12 VDC Auxiliary
13			14		
15			16		
17			18		
19			20	MPR0/	Memory Protect
21			22		
23			24		
25			26		
27	**M1/	Status of CPU Fetch Cycle	28		
29	PAR ERR/	Parity Error	30		
31			32		
33			34		
35			36		
37			38		
39			40		
41			42		
43			44		
45			46		
47			48		
49			50		
51			52		
53			54		
55			56	EXRES/	External Reset
57	LPTP	Low Parity Test Point	58	CLTP	Clear Test Point
59	HPTP	High Parity Test Point	60		

*Where: Auxiliary power is provided by backup battery source.

**Where: M1/ = Machine state 1 of 8080A CPU.

Note: Uncommitted pins are reserved for future use.

TABLE J-8 SLAVE PROCESSOR/MEMORY CONNECTOR P2 PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1		2	
3		4	
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21		22	
23		24	SIOD
25	RESET	26	
27		28	
29		30	
31		32	
33		34	
35		36	TPMPT/
37		38	HLDA/
39		40	
41		42	
43		44	
45		46	LATCH/
47		48	CL1/
49		50	CL2/
51		52	
53		54	XCLK
55		56	QMBRQ/
57		58	MRQ
59		60	WIM

TABLE J-9 BLC-8222 CONNECTOR P2, PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	DBØ	2	—
3	DB1	4	—
5	DB2	6	—
7	DB3	8	—
9	DB4	10	—
11	DB5	12	—
13	DB6	14	—
15	DB7	16	BASE=/
17	CMD BASE +1	18	CMD BASE +2
19	—	20	—
21	—	22	—
23	—	24	—
25	—	26	—
27	—	28	—
29	—	30	—
31	—	32	—
33	—	34	—
35	—	36	—
37	—	38	—
39	—	40	BPRN/
41	—	42	—
43	—	44	BREQ/
45	—	46	—
47	DISABLE BASE	48	—
49	—	50	—
51	—	52	—
53	—	54	—
55	—	56	—
57	—	58	—
59	—	60	—

TABLE J-10 BLC-8222 CONNECTOR J2, PIN ASSIGNMENTS

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	ABOVE TRK 43/
3		4	
5		6	
7		8	ABOVE TRK 43/
9		10	
11		12	DISK CHANGE/
13		14	SIDE SELECT/
15		16	
17		18	HEAD LOAD/
19		20	INDEX/
21		22	READY/
23		24	
25		26	DRIVE SELECT 1/
27		28	DRIVE SELECT 2/
29		30	DRIVE SELECT 3/
31		32	DRIVE SELECT 4/
33		34	DIRECTION SELECT/
35		36	STEP/
37		38	WRITE DATA/
39		40	WRITE GATE/
41		42	TRACK ØØ/
43		44	WRITE PROTECT/
45		46	READ DATA/
47		48	
49	GND	50	

TABLE J-11 BLC-8222 CONNECTOR J3, PIN ASSIGNMENTS (MINIATURE DISK DRIVES 1 AND 3)

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	
3		4	
5		6	
7		8	INDEX/
9		10	DRIVE SELECT 1/
11		12	DRIVE SELECT 2/
13		14	
15		16	MOTOR ON/
17		18	DIRECTION SELECT/
19		20	STEP/
21		22	WRITE DATA/
23		24	WRITE GATE/
25		26	TRACK ØØ/
27		28	WRITE PROTECT/
29		30	READ DATA/
31		32	SIDE SELECT/
33	GND	34	

TABLE J-12 BLC-8222 CONNECTOR J4, PIN ASSIGNMENTS (MINIATURE DISK DRIVES 3 AND 4)

COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	
3		4	
5		6	
7		8	INDEX/
9		10	DRIVE SELECT 3/
11		12	DRIVE SELECT 4/
13		14	
15		16	MOTOR ON/
17		18	DIRECTION SELECT/
19		20	STEP/
21		22	WRITE DATA/
23		24	WRITE GATE/
25		26	TRACK ØØ/
27		28	WRITE PROTECT/
29		30	READ DATA/
31		32	SIDE SELECT/
33	GND	34	

Appendix A

EQUIPMENT OUTLINE DRAWINGS

The Equipment Outline Drawing for the MSC-6601/MSC-6605 Rack-Mount Computer Systems are shown on pages A-2 through A-7/A-8.

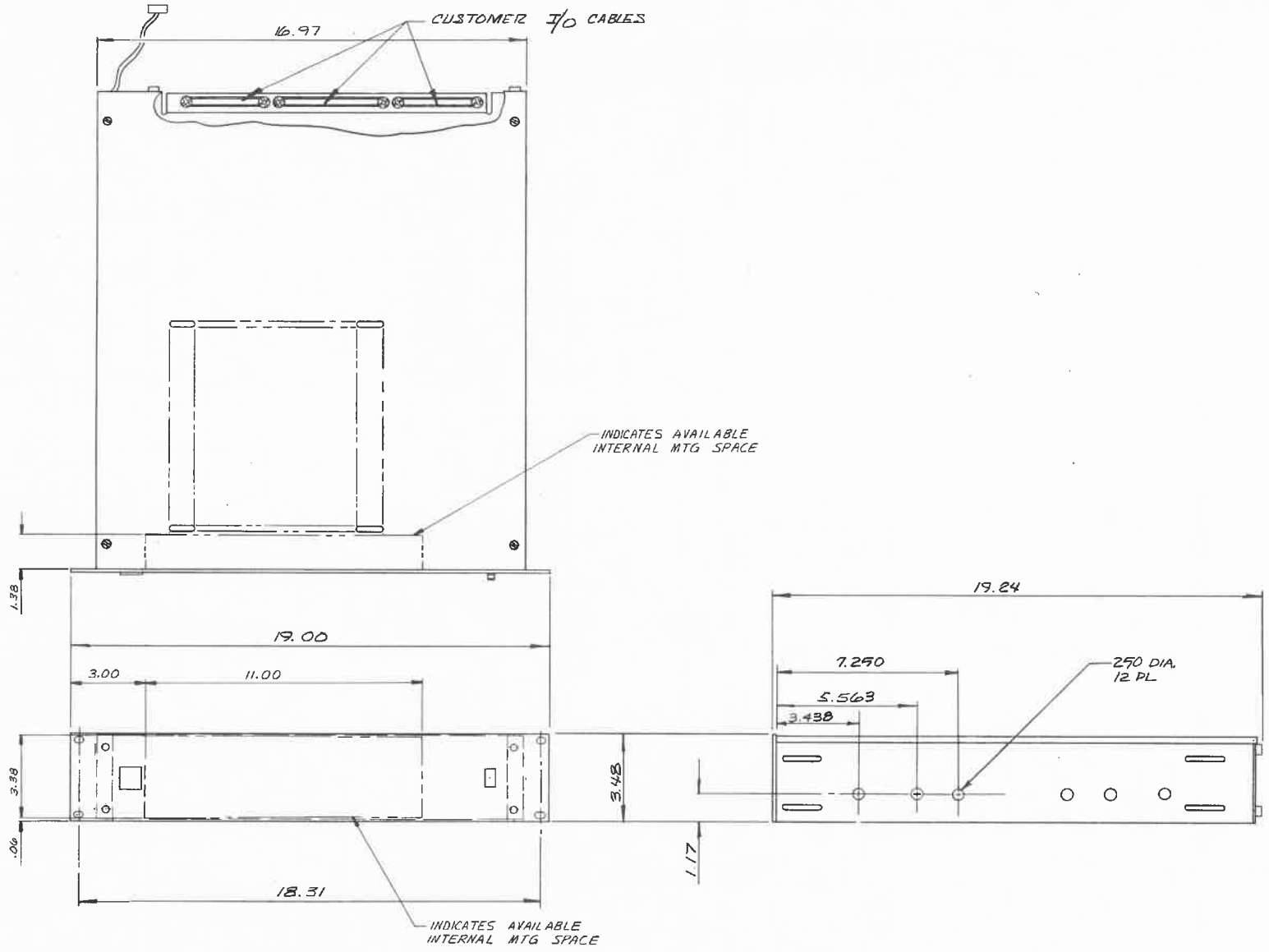


Figure A-1 4-Slot Module Outline Drawing

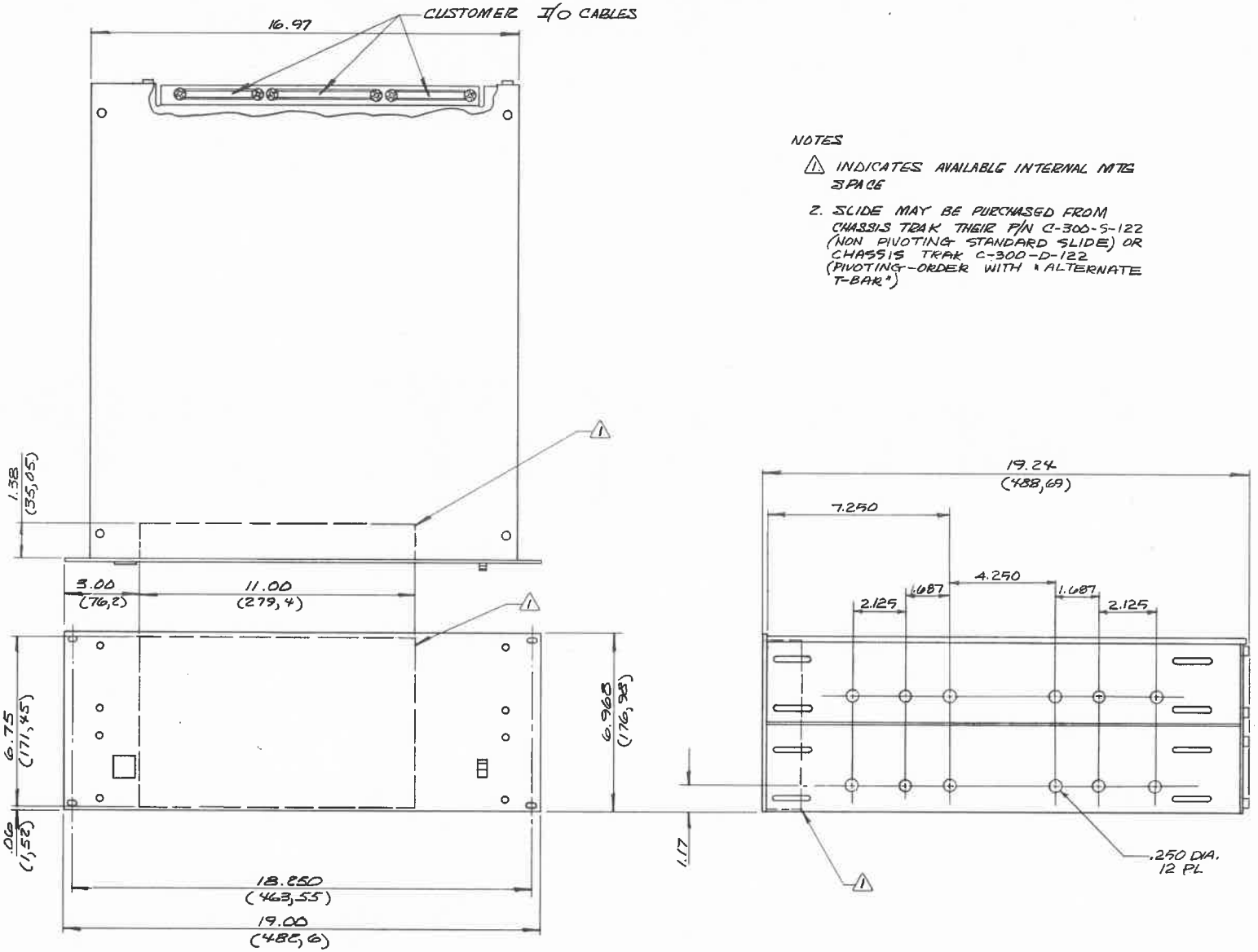


Figure A-2 8-Slot Module Outline Drawing

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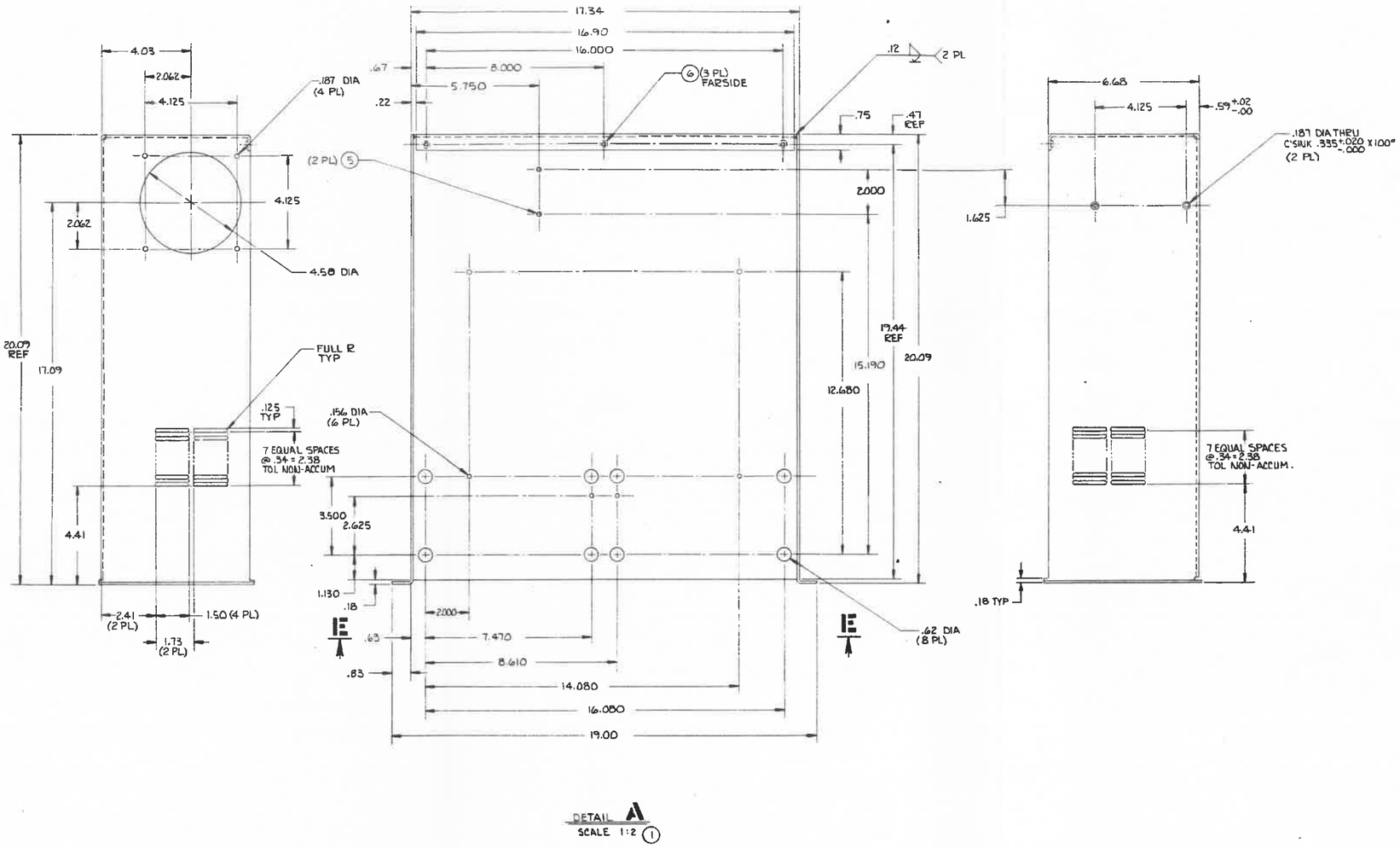

DETAIL A
SCALE 1:2 (1)

Figure A-3 Flexible Disk Drive Module Outline Drawing

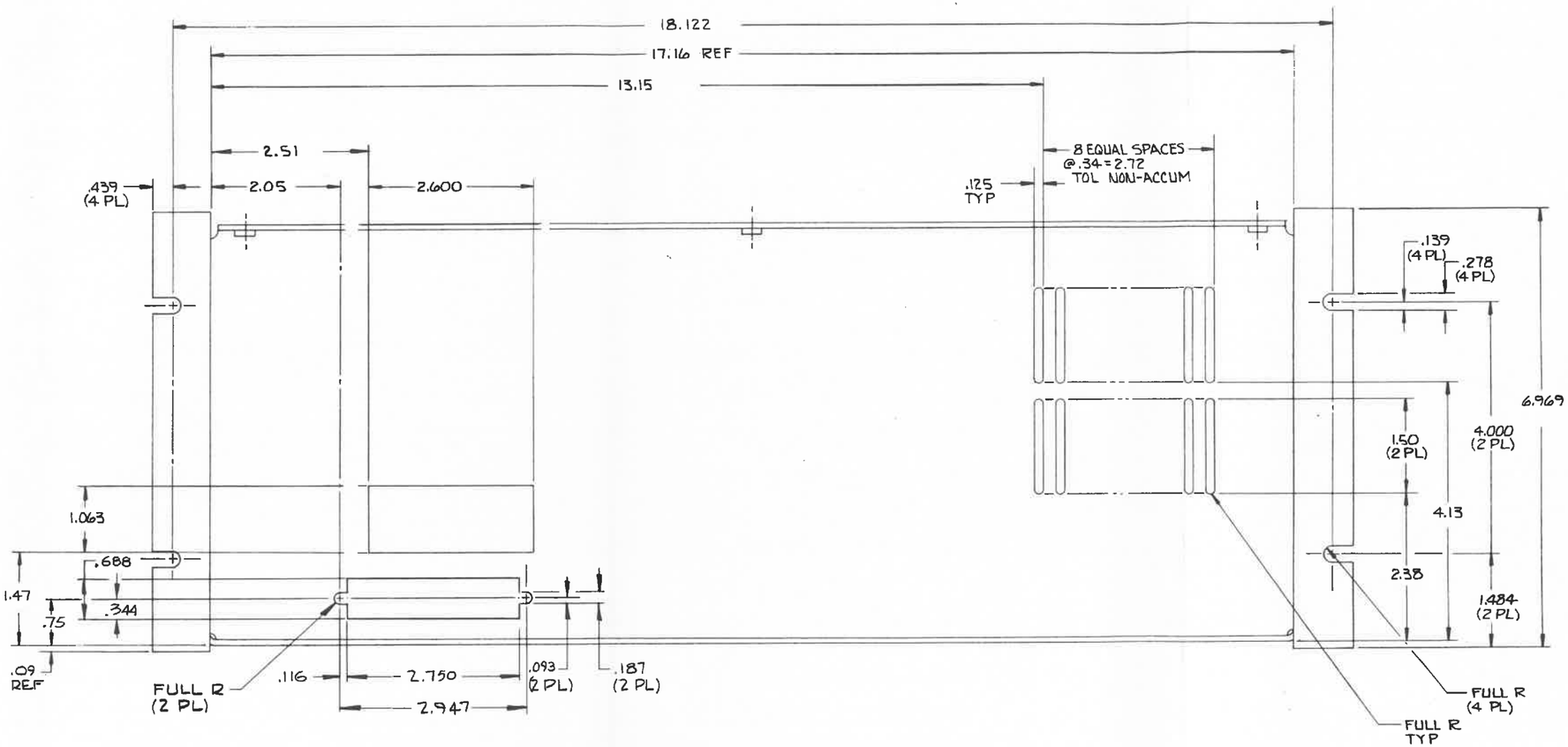

Figure A-4 Flexible Disk Drive Module Outline Drawing

Appendix B

BOARD JUMPER CONFIGURATIONS

The Board Jumper Configurations for the MSC-6601/MSC-6605 Rack-Mount Computer Systems are shown on pages B-3/B-4 through B-7/B-8.

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APPENDIX B
JUMPER CONFIGURATIONS

JUMPER NO.		STATE (NATIONAL FACTORY INSTALLED)	FIELD AREA	FUNCTION
WX	1-2	Closed	1	Enable fail safe timer.
W2		Open	8	
W3	1-2	Closed	8	TXD for data set (#2 8251).
W4	1-2		5	DTR for data set (#1-8251).
W5	4-7		5	TXD for data set (#1-8251).
	5-6		5	RTS for data set (#1-8251).
W6	1-2		8	DTR for data set (#2 8251).
	3-4		8	RTS for data set (#2 8251).
W7	1-2		2	Port E4, Set 8303 as receiver.
	3-16		2	Enable timer gate.
	4-17		2	Enable timer gate.
	5-18		2	Port E7 to socket.
	6-19		2	Port E7 to socket.
	7-20		2	Port E7 to socket.
	8-21		2	Port E7 to socket.
	9-22		2	Port E6 to socket.
	10-23		2	Port E6 to socket.
	11-24		2	Port E6 to socket.
	12-25		2	Port E6 to socket.
W8	1-2		3	Supply 1.841 MHz to CLK Input of 8253.
W9	1-2		4	Port E8, set 8304 as receiver
	5-16		4	Port E8 to socket.
	6-17		4	Port E8 to socket.
	7-18		4	Port E8 to socket.
	8-19		4	Port E8 to socket.
	9-20		4	Port EA to socket.
	10-21		4	Port EA to socket.
	11-22		4	Port EA to socket.
	12-23		4	Port EA to socket.
W10	4-8		4	CTS for data set USART #1.
	5-9		4	RXD for data set USART #1.
	6-10		4	DSR for data set USART #1.
W11	1-2	Closed	6	CTS to RTS of USART #1.
W12		Open	6	
W13	1-2	Closed	6	RTS to CTS of USART #1.
W14		Open	7	
W15		Open	7	
W16	1-2	Closed	7	CTS to RTS of USART #2.
W17	4-8		9	CTS for data set USART #2.
	5-9		9	RXD for data set USART #2.
	6-10		9	DSR for data set USART #2.
W18	1-2		10	Supply 18.432 MHz to Bus CLK logic.
W19	1-2		13	Supply 22.1184MHz to Z80 CLK logic.
W20	1-2		11	Supply 1.841 MHz to 8251.
W21	2-3		12	Connects baud CLK to TXC #1 USART (with 4-3 open)
	6-7		12	Connects baud CLK to RXC #2 USART (with 7-8 open)
W22	2-3		12	Connects baud CLK to TXC #2 USART (with 4-3 open)
	6-7		12	Connects baud CLK to RXC #2 USART (with 7-8 open)
W23	1-2	Closed	12	RTS to CTS of USART #2.
W24	7-17	Closed	13	PROM INTR to master interrupt controller IR7.
	8-18		13	Printer INTR to master interrupt controller IR6.
	9-19		13	#2 TXR INTR to master interrupt controller IR5.
	10-20		13	#1 TXR INTR to master interrupt controller IR4.
	11-21		13	Slave 8259 INTR to master interrupt controller IR3.
	12-22		13	Counter INTR to master interrupt controller IR2.
	13-23		13	#2 RXR INTR to master interrupt controller IR1.
	14-24		13	#1 RXR INTR to master interrupt controller IR0.
	15-25		13	NMI disenabled.
W25	1-2		14	Supply C CLK to MULTIBUS (remove when more than one master is used).
	4-3		14	Supply B CLK to bus controller & MULTIBUS.
W26	1-2		14	Connects BPRO/ to MULTIBUS.
W27	1-2		15	Connects CB REQUEST/ to ground.
W28	1-9		15	INT2 from MULTIBUS connects to slave I.C. IR2.
	2-10		15	INT6 from MULTIBUS connects to slave I.C. IR6.
	3-11		15	INT1 from MULTIBUS connects to slave I.C. IR1.
	4-12		15	INT5 from MULTIBUS connects to slave I.C. IR5.
	5-13		15	INT0 from MULTIBUS connects to slave I.C. IR0.
	6-14		15	INT4 from MULTIBUS connects to slave I.C. IR4.
	7-15		15	INT3 from MULTIBUS connects to slave I.C. IR3.
	8-16	Closed	15	INT7 from MULTIBUS connects to slave I.C. IR7.

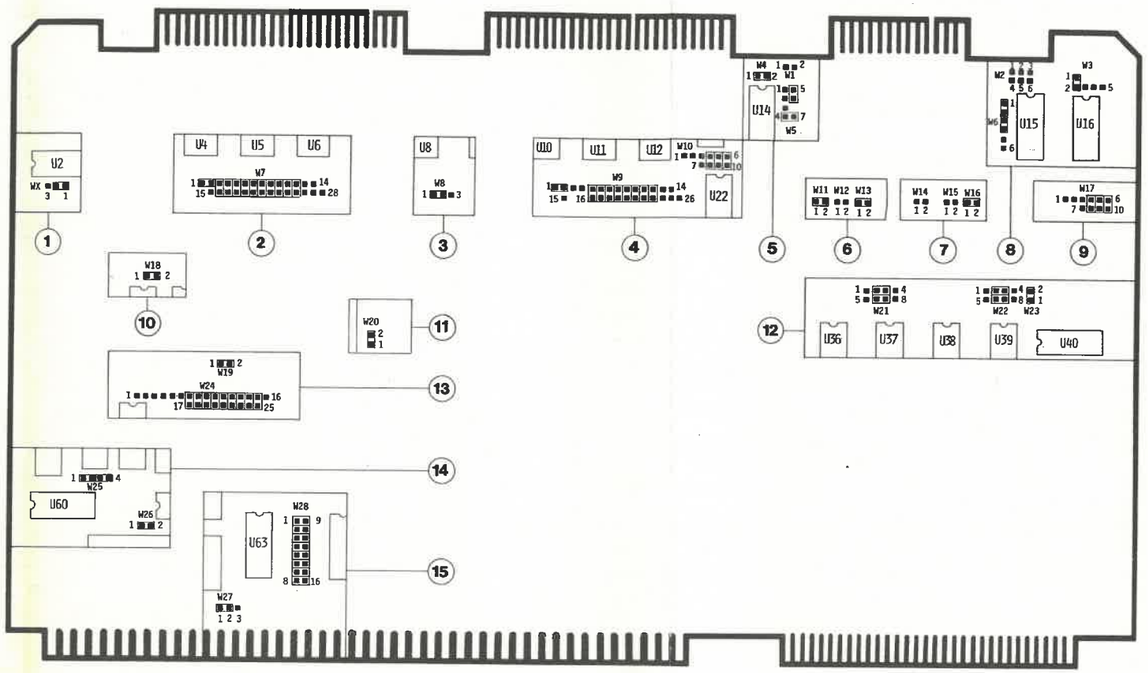

Figure B-1 Jumper Configuration for System Processor Board

JUMPER NO.	STATE (NATIONAL FACTORY INSTALLED)	FIELD AREA	FUNCTION
W1 A-C	Closed	4	Selects timing signal for refresh address counter.
C-B	Open	4	
W2 A-C	Closed	4	Selects timing signal for latching data in/out RAM.
C-B	Open	4	
W3 A-C	Closed	4	Selects timing signal for refresh enable pulse.
C-B	Open	4	
W4 A-C	Closed	4	Selects timing signal for row enable pulse.
C-B	Open	4	
W5 A-C	Closed	4	Selects timing signal for row enable pulse.
C-B	Open	4	
W6 A-C	Closed	4	Selects timing signal for write an row address strobe.
C-B	Open	4	
W7 A-C	Closed	4	Selects timing signal for row address strobe.
C-B	Open	4	
W8 A-C	Closed	4	Selects timing signal for row address strobe.
C-B	Open	4	
W9 A-C	Closed	4	Selects timing signal for column address strobe.
C-B	Open	4	
W10 A-C	Closed	4	Selects timing signal for column address strobe.
C-B	Open	4	
W11 A-C	Closed	4	Selects timing signal for read/write refresh cycle time.
C-B	Open	4	
W12 A-C	Closed	4	Controls up/down counter that generates timing signals.
C-B	Open	4	
W13 A-C	Closed	4	Selects timing signal for system XACK pulse.
C-B	Open	4	
W14 A,B,C	Open	4	Selects timing signal for system AACK.
W15 B-C	Open	4	
W15A-W16	Closed	4	
E1-E9	Closed	2	
E1-E10	Open	2	
E2-E12	Closed	2	
E2-E11	Open	2	Selects 16K bank address boundries. This configuration selects 0-16K, 16K-32K, 32K-48K, and 48K-64K boundries.
E3-E14	Closed	2	
E3-E13	Open	2	
E4-E15	Closed	2	
E4-E16	Open	2	
E5-E21	Closed	2	
E5-E22	Open	2	
E5-E23	Open	2	
E5-E24	Open	2	
E6-E25	Open	2	
E6-E26	Open	2	Selects 64K page address boundries. This configuration selects page 0 (address range 00000-0FFFFH).
E6-E27	Open	2	
E6-E28	Open	2	
E7-E17	Closed	5	
E7-E19	Open	5	
E8-E18	Closed	5	
E8-E20	Open	5	
E29-E30	Closed	6	Selects write enable signal.
E29-E31	Open	6	
E32-E33	Closed	1	(wirewrap)
E34-E35	Closed	1	(wirewrap) Supplies +5, -5, and -12V to P2 connector.
E36-E37	Closed	1	(wirewrap)
E38-E41	Closed	3	
E38-E43	Open	3	
E38-E45	Open	3	Selects source of RAM Address Bit 5 during refresh.
E39-E40	Closed	3	
E39-E42	Open	3	
E39-E44	Open	3	
E50-E51	Closed	5	Enables serial Bus Priority.
E52-E53	Open	5	Enables +10V voltage divider.
TP1-TP2	Closed	7	Selects XTAL Clock.
TP1-TP3	Open	7	

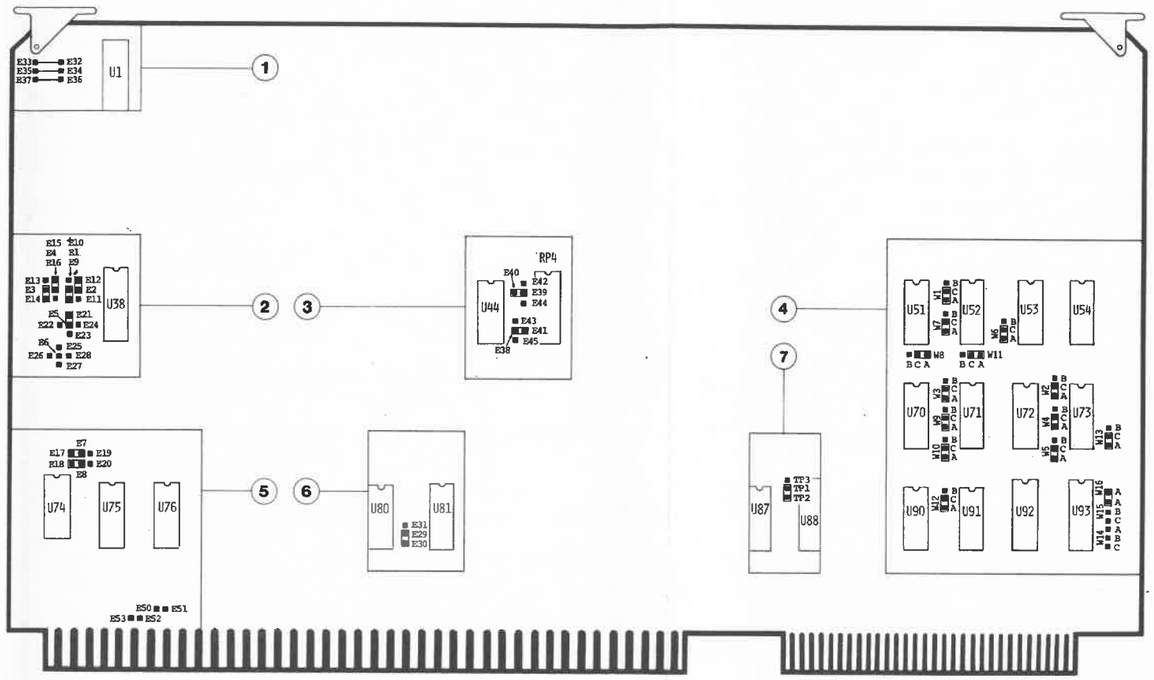

Figure B-2 Jumper Configuration for BLC-064 RAM Board

JUMPER NO.	STATE (NATIONAL FACTORY INSTALLED)	FIELD AREA	FUNCTION
W1 and W2	Open	2	Permits user to select miniature drive type. W1 open and W2 closed allows standard size drive to operate in system. W1 closed and W2 open allows miniature size drive to operate in system.
	Closed	2	
W3	Open (-002)	2	Permits user to select double- or single-sided drive type. W3 closed allows double-sided drive type to operate in system. W3 open allows single-sided drive to operate in system.
	Closed (-001)	2	
W4 and W5	Closed	5	Permits Bus Priority Out (BPRO/) signal to be enabled for use with BLC 80/10 CPU board or other types of Series 80 CPU boards. W4 closed and W5 open enables BPRO/ signal to establish serial priority for all Series 80 CPU boards (except BLC-80/10) to gain access to system bus. W4 open and W5 closed allows BLC 80/10 CPU board to operate in system by shorting BPRO/ and BREQ/ signals.
	Open	5	
S1-1	Off	3	S1 sets interrupt output to one of eight system bus interrupt lines (INTU-INT7). This configuration selects INT5.
S1-2	Off	3	
S1-3	Off	3	
S1-4	Off	3	
S1-5	Off	3	
S1-6	On	3	
S1-7	Off	3	
S1-8	Off	3	
S2-1	Off	3	S2 sets Base Address. This configuration sets base address equal to 70H.
S2-2	On	3	
S2-3	On	3	
S2-4	On	3	
S2-5	Off	3	
Z1-1 to Z1-2	Closed	6	Permits external test clock frequency to be applied to INS8224 Clock Generator and Driver Chip. Z1-1 to Z1-2 allows internal 16 MHz clock, Y1 to operate in system. Z1-1 to Z1-3 bypasses internal clock and allows user to apply external test clock frequency to system.
Z2-1 to Z2-2*	Closed	1	Z2 through Z5 reserved for future use.
Z3-1 to Z3-2*	Closed	1	
Z4-1 to Z4-2*	Closed	1	
Z5-1 to Z5-2**	Closed	4	

* Z2 through Z4 available on 980305804-000 Rev. H and higher only.
** Z5 available on 980305804-000 Rev. J and higher only.

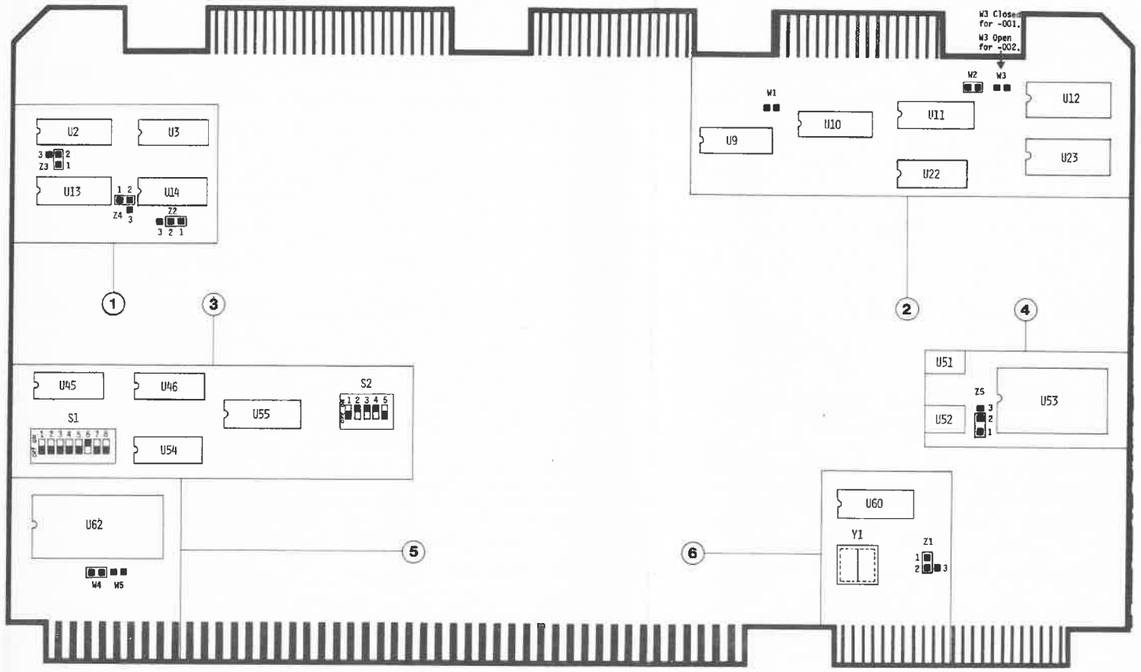

Figure B-3 Jumper Configuration for BLC-8222 Disk Controller Board

Appendix C

BOARD ASSEMBLIES

The Board Assemblies for the MSC-6601/MSC-6605 Rack-Mount Computer Systems are shown on pages C-3/C-4 through C-7/C-8.

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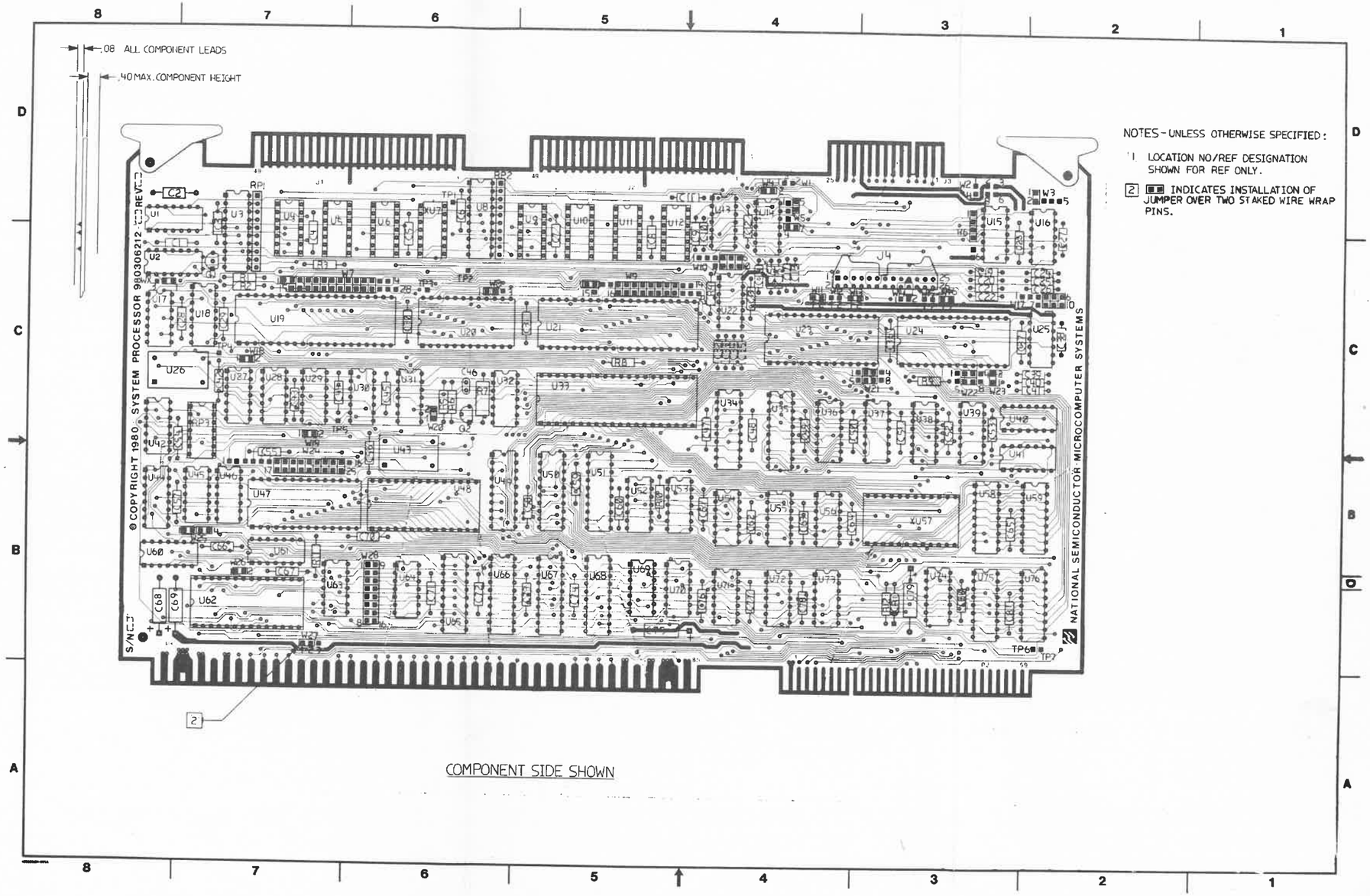

.08 ALL COMPONENT LEADS
.40 MAX. COMPONENT HEIGHT
NOTES - UNLESS OTHERWISE SPECIFIED:
1 LOCATION NO/REF DESIGNATION SHOWN FOR REF ONLY.
2 ■■ INDICATES INSTALLATION OF JUMPER OVER TWO STAKED WIRE WRAP PINS.
© COPYRIGHT 1980, SYSTEM PROCESSOR 880306212 REV.
S/N
NATIONAL SEMICONDUCTOR MICROCOMPUTER SYSTEMS
COMPONENT SIDE SHOWN

Figure C-1 Assembly Drawing for System Processor Board

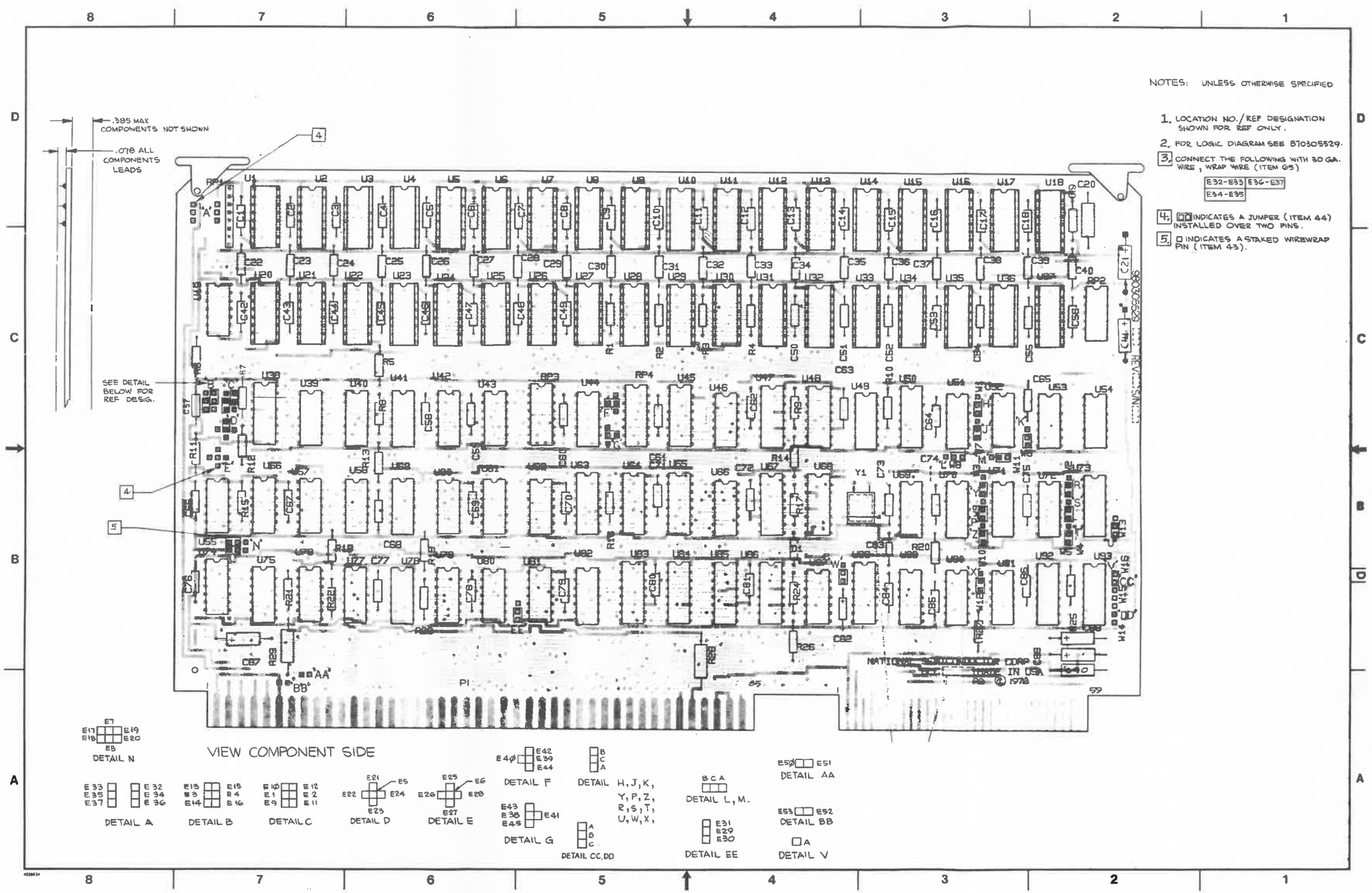


Figure C-2 Assembly Drawing for BLC-064 RAM Board

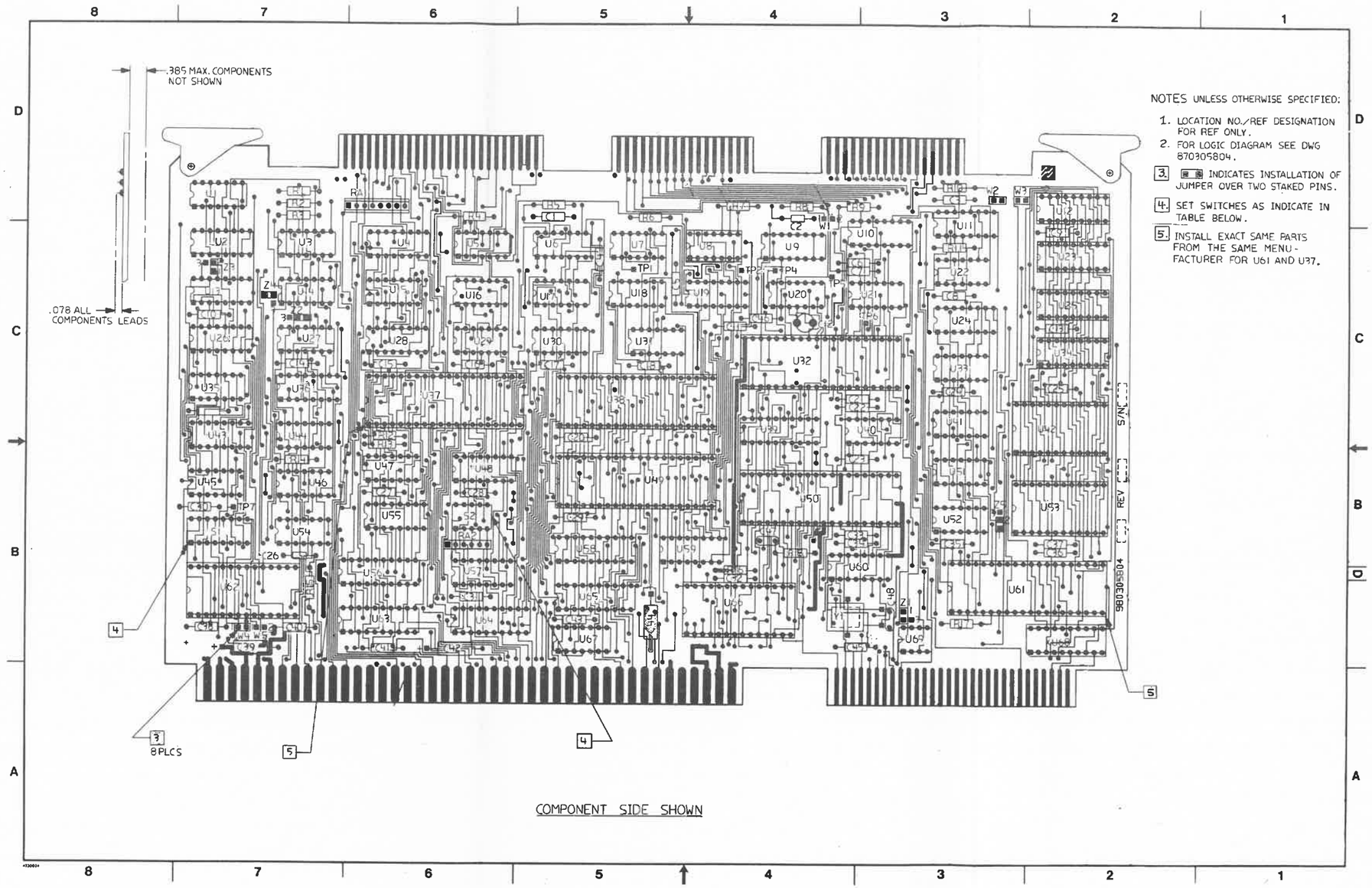

.385 MAX. COMPONENTS NOT SHOWN
.078 ALL COMPONENTS LEADS
NOTES UNLESS OTHERWISE SPECIFIED:
1. LOCATION NO./REF DESIGNATION FOR REF ONLY.
2. FOR LOGIC DIAGRAM SEE DWG 870305804.
3. INDICATES INSTALLATION OF JUMPER OVER TWO STAKED PINS.
4. SET SWITCHES AS INDICATE IN TABLE BELOW.
5. INSTALL EXACT SAME PARTS FROM THE SAME MENU-FACTURER FOR U61 AND U37.
8 PLCS
COMPONENT SIDE SHOWN
S/N
REV
870305804

Figure C-3 Assembly Drawing for BLC-8222 Disk Controller Board

Appendix D

SYSTEM PROCESSOR LOGIC DIAGRAMS

The Logic Diagrams for the MSC-6601/MSC-6605 System Processor Board are shown on page D-2 through D-12.

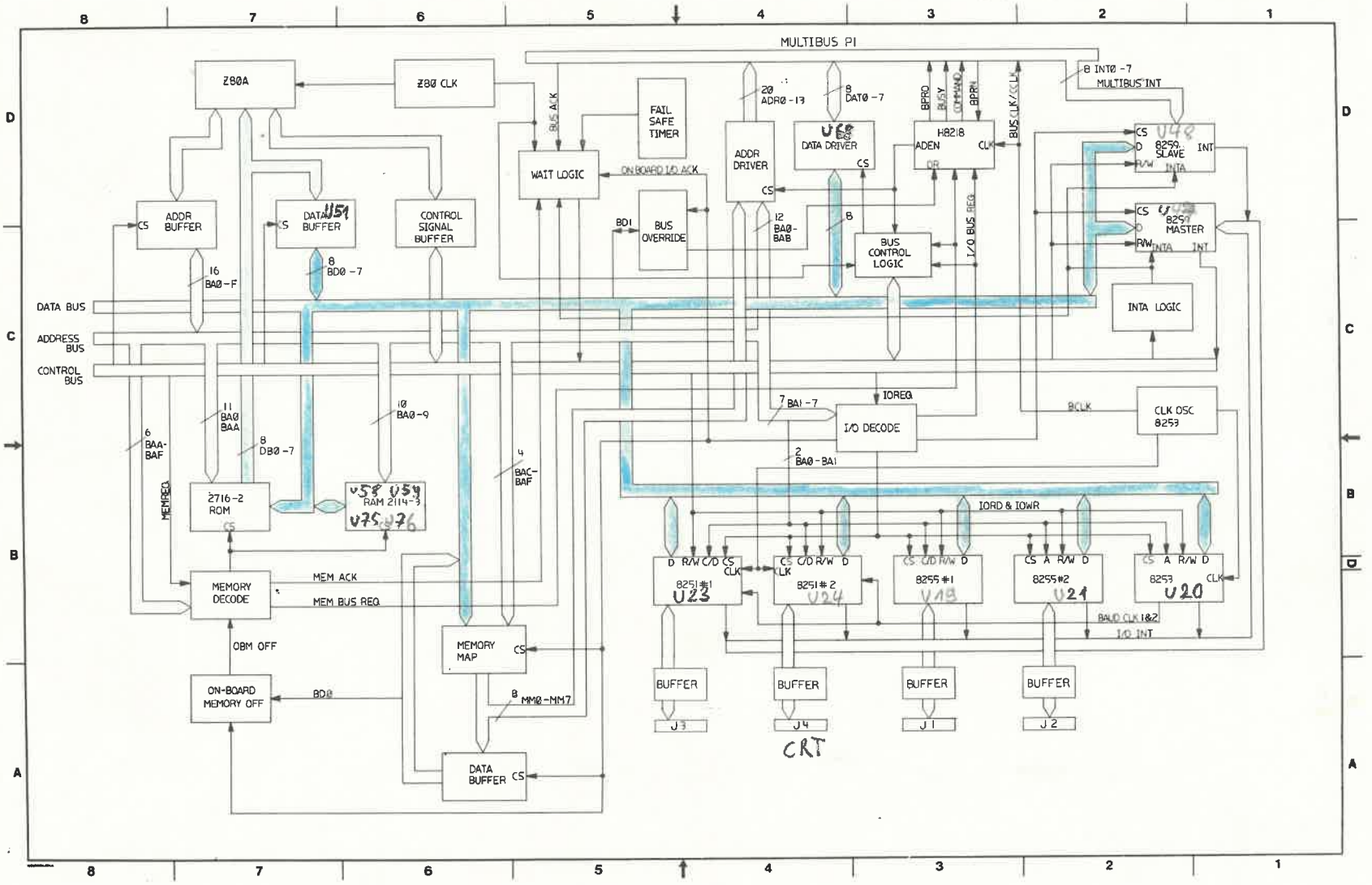
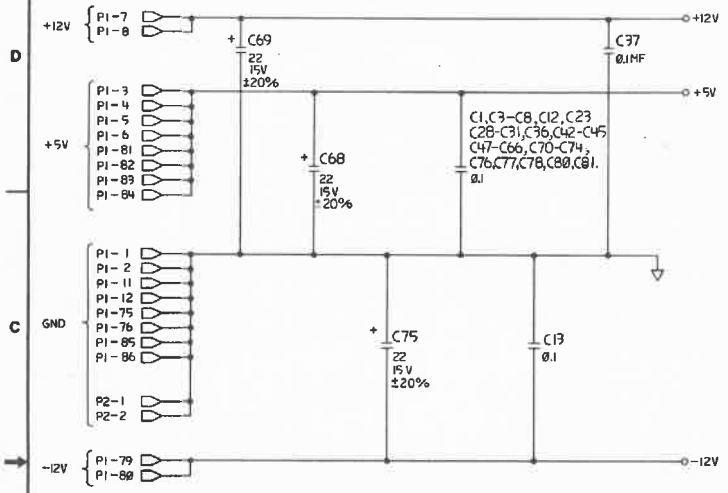


Figure D-1 Logic Diagrams for System Processor Board



TYPE	+12V	+5V	GND	-5	-12V	REF DES	UNUSED OUTPUTS
74S74		14	7			U1,U27,U31,U42,	
74S08		14	7			U2,U53,U60,U73	U60-11
8303		20	10			U3,U68	
SOCKET		14	7			XU7	
1489		14	7			U13 - U16	
74S32		14	7			U17,U55,U56,U69 U70	U17-11
8602		16	8			U18	U18-19
8255		26	7			U19,U21	
8253		24	12			U20	
1488	14		7		1	U22,U25	
8251		26	4			U23,U24	
74178		14	7			U28,U29	
74S260		14	7			U30	
74S04		14	7			U32,U40,U61,U63, U64	U32-8,12.U40-12 U61-6,10,12
Z80A		11	20			U33	
74S240		20	10			U34,U66,U67	U66-3
81LS98		20	10			U35	
74S189		16	8			U36,U37	
74S139		16	8			U38	
74S00		14	7			U41,U54,U72	U72-6
74S140		14	7			U45	
74S38		14	7			U46	U46-3,11
8259		28	14			U47,U48	
74S373		20	10			U49,U50	
8304		20	10			U51,U8	
74LS14		14	7			U52	U52-2,10,12
2716-2		24	12			U57	
2114-3		18	9			U58,U59,U75,U76	
8218		28	14			U62	
74S244		20	10			U65	
74S11		14	7			U71	
74S02		14	7			U74	
74S175		16	8			U44	U44-14,15
7408		14	7			U4,U5	
7438		14	7			U6,U9,U11,U12	
BLC902						U10	
74S138		16	8			U39	

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
2. ALL CAPACITOR VALUES ARE IN MICROFARAD +80%,-20%.
3. ALL INTEGRATED CIRCUITS ARE 74XXX SERIES.
4. * DENOTES CUSTOMER INSTALLED CAPACITORS

Figure D-1 Logic Diagrams for System Processor Board

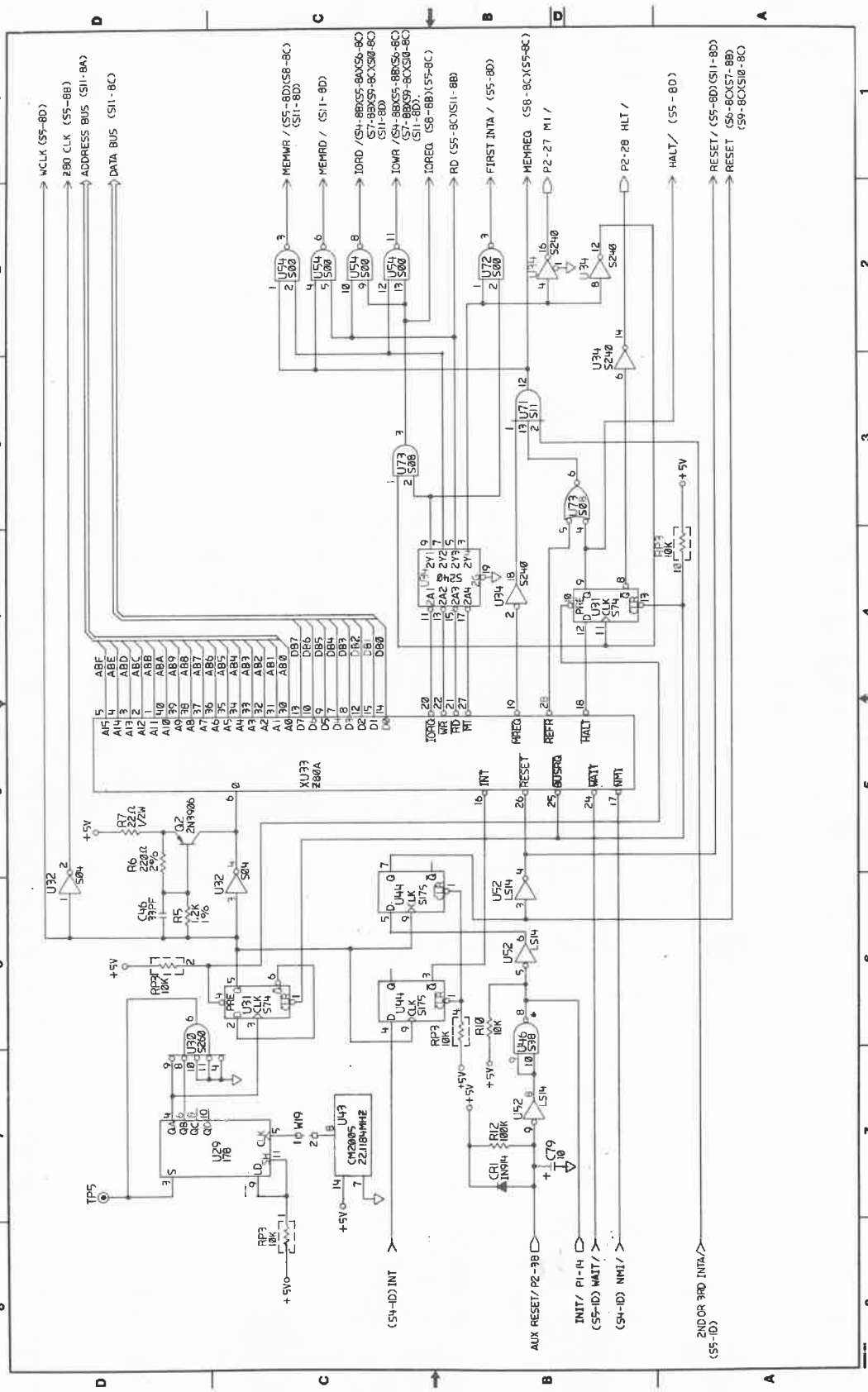


Figure D-1 Logic Diagrams for System Processor Board

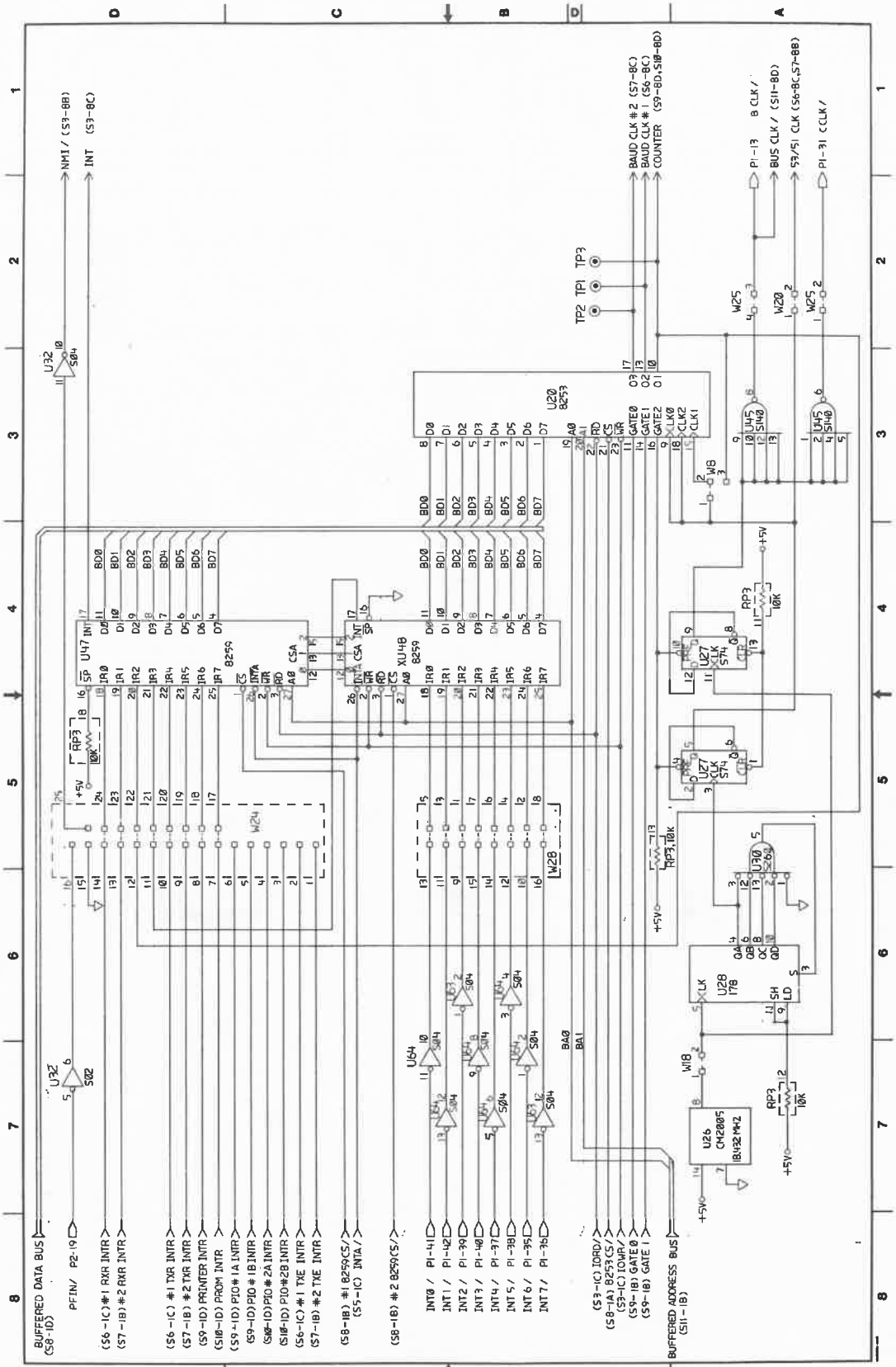


Figure D-1 Logic Diagrams for System Processor Board

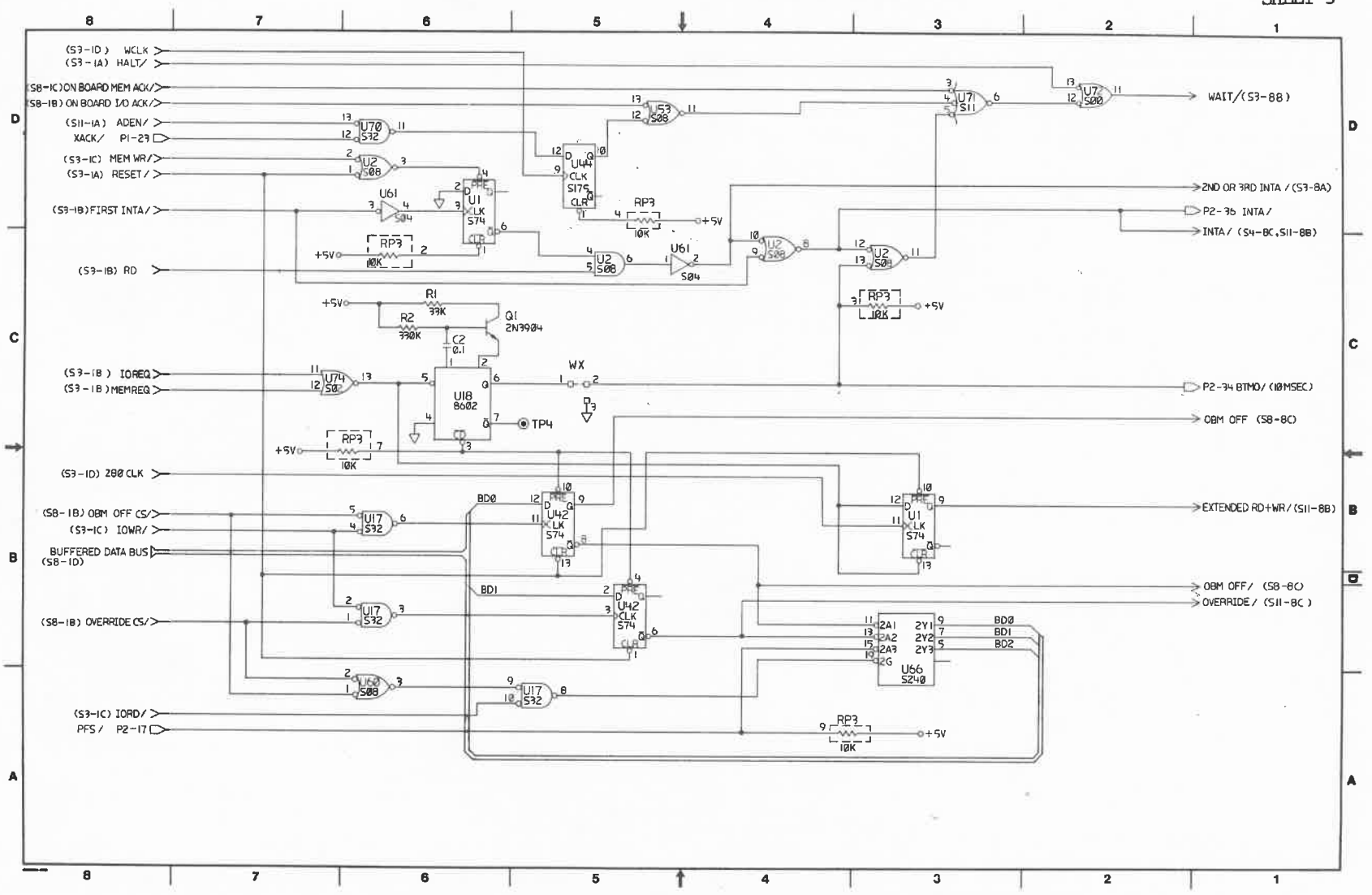


Figure D-1 Logic Diagrams for System Processor Board

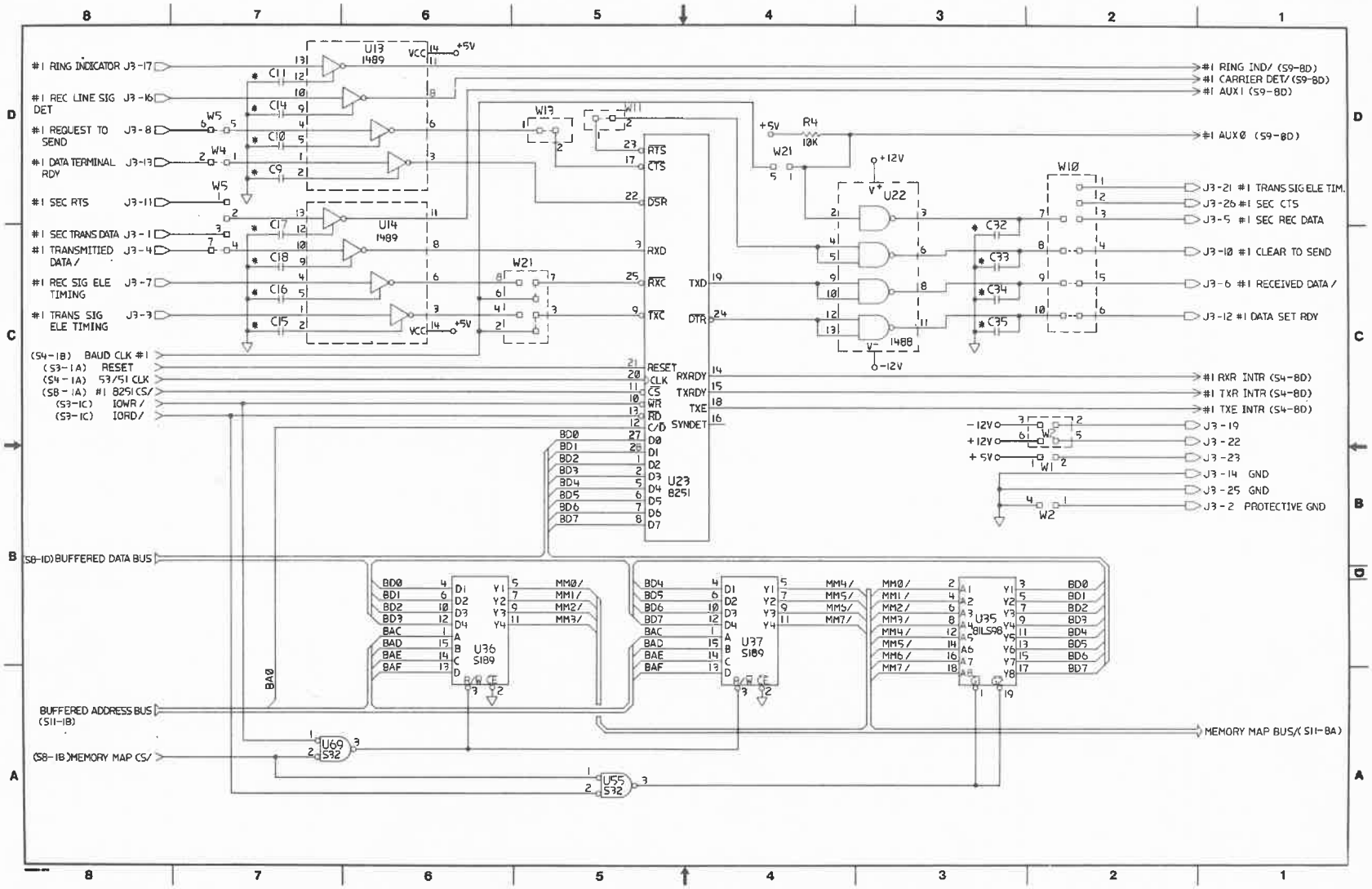


Figure D-1 Logic Diagrams for System Processor Board

CRT

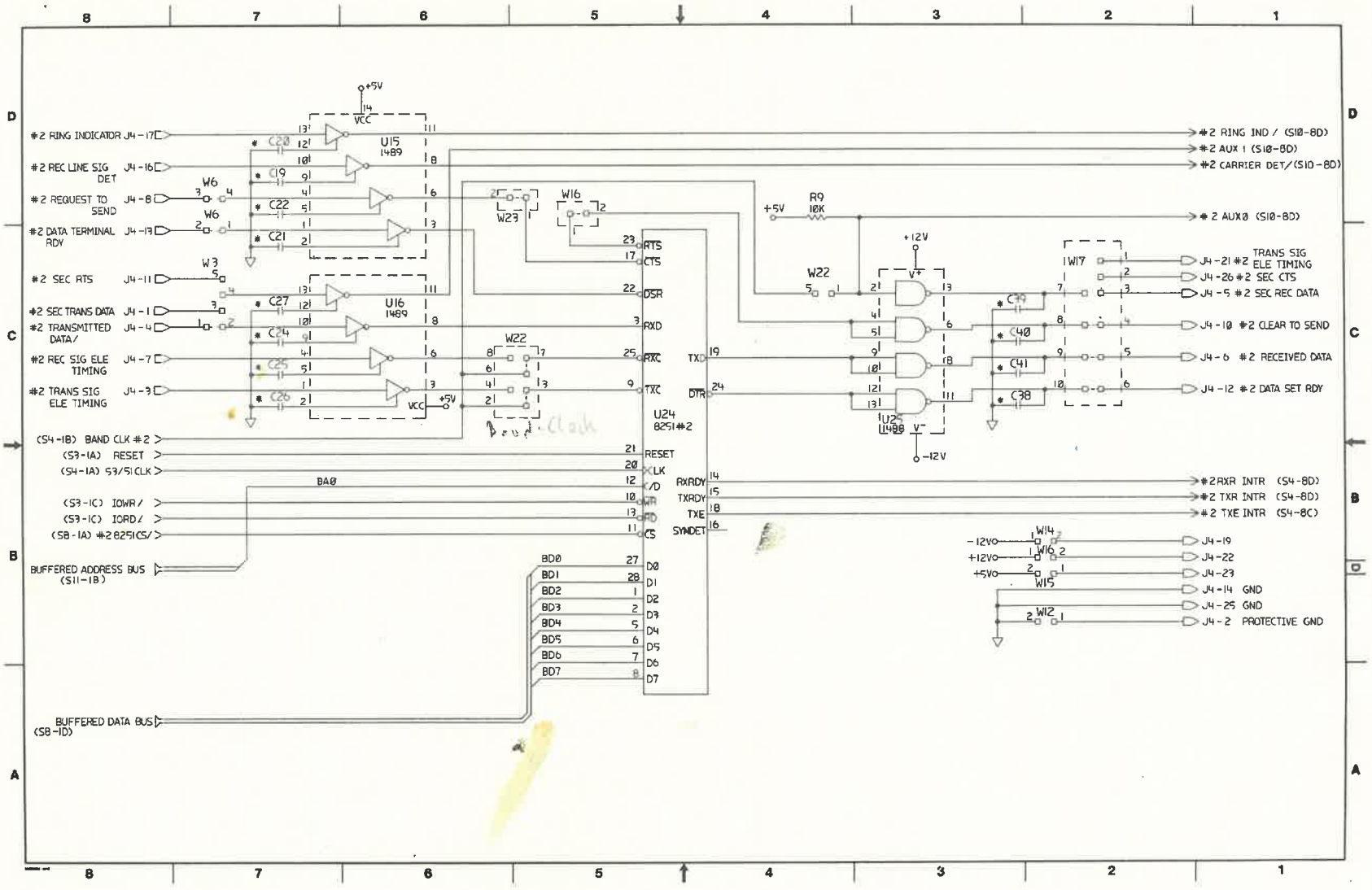


Figure D-1 Logic Diagrams for System Processor Board

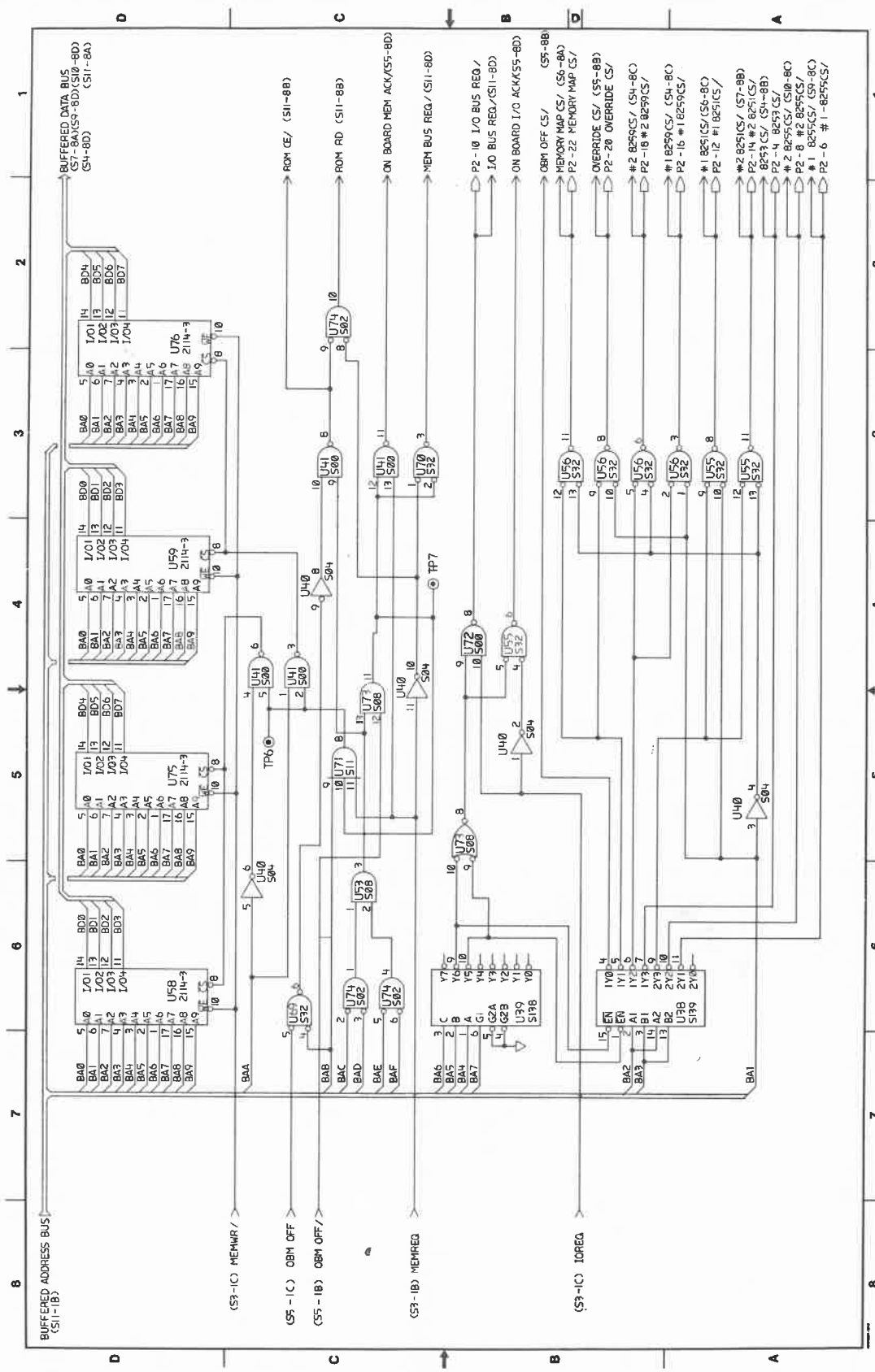


Figure D-1 Logic Diagrams for System Processor Board

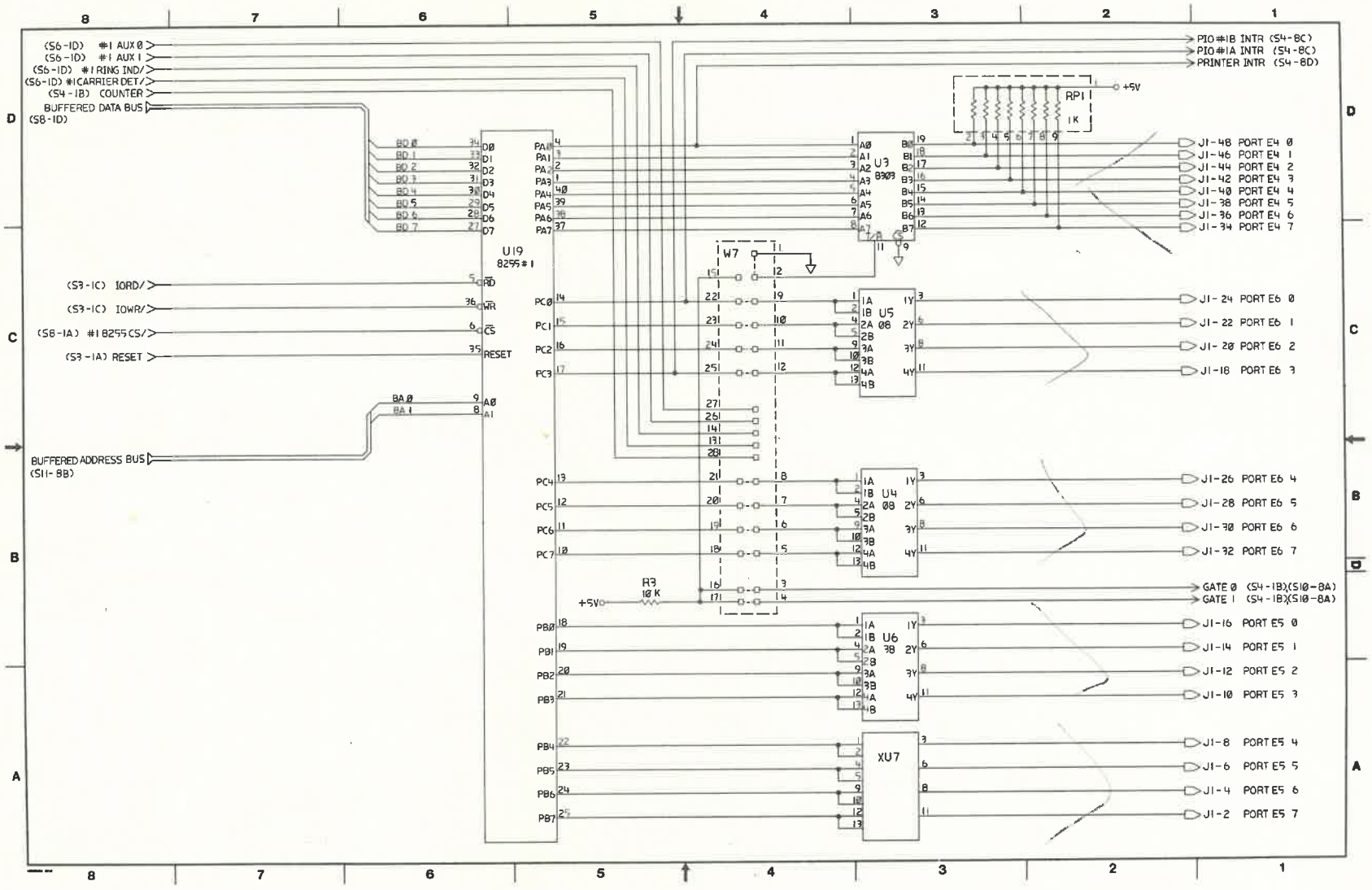


Figure D-1 Logic Diagrams for System Processor Board

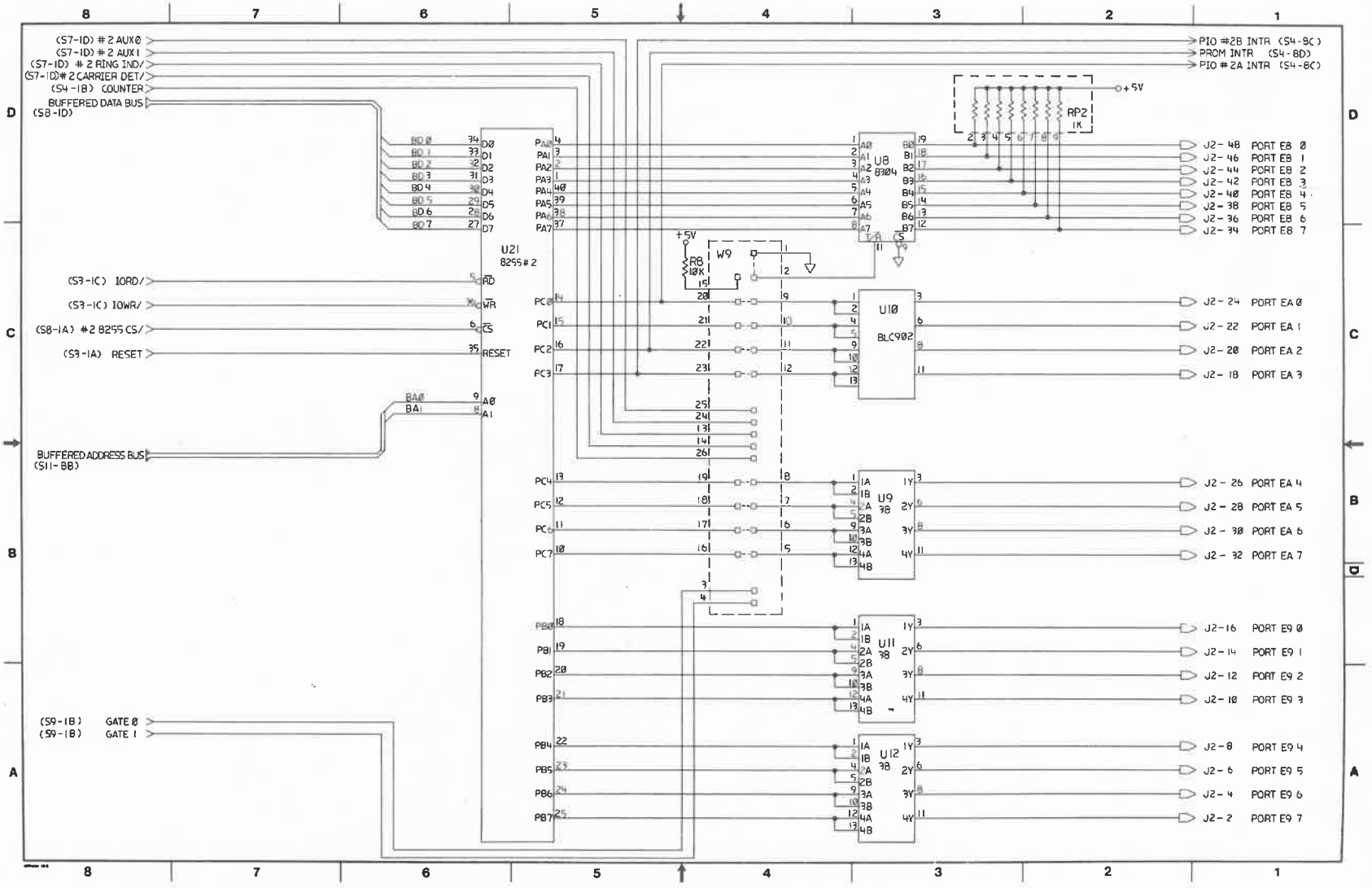


Figure D-1 Logic Diagrams for System Processor Board

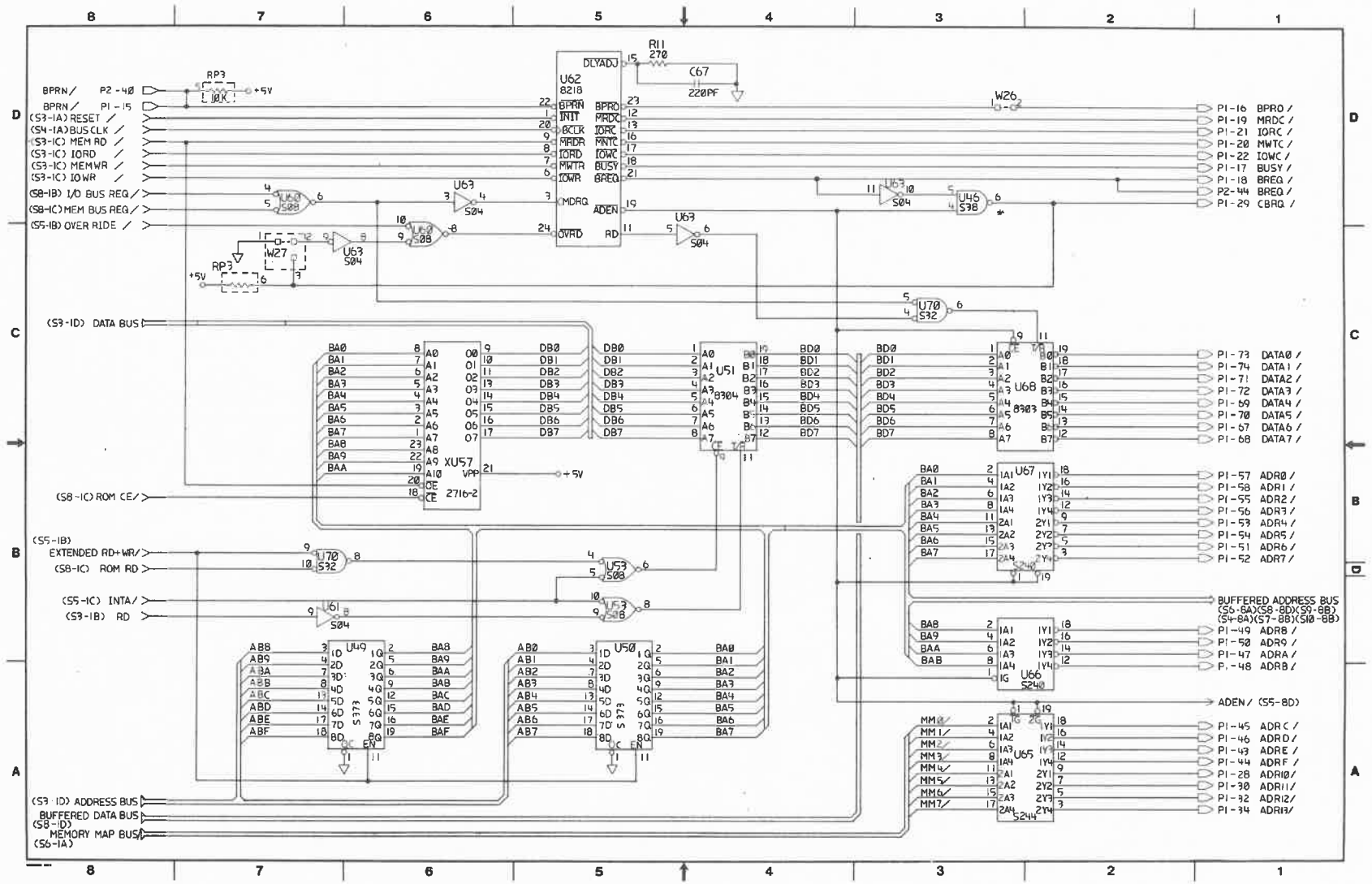


Figure D-1 Logic Diagrams for System Processor Board

Appendix E

WIRING DIAGRAMS

The Wiring Diagrams for the MSC-6601 4-slot and MSC-6605 8-slot Rack Mount Modules are shown on pages E-2 and E-3/E-4, respectively. The Wiring Diagram for the MSC-6601/MSC-6605 Floppy Module is shown on page E-5.

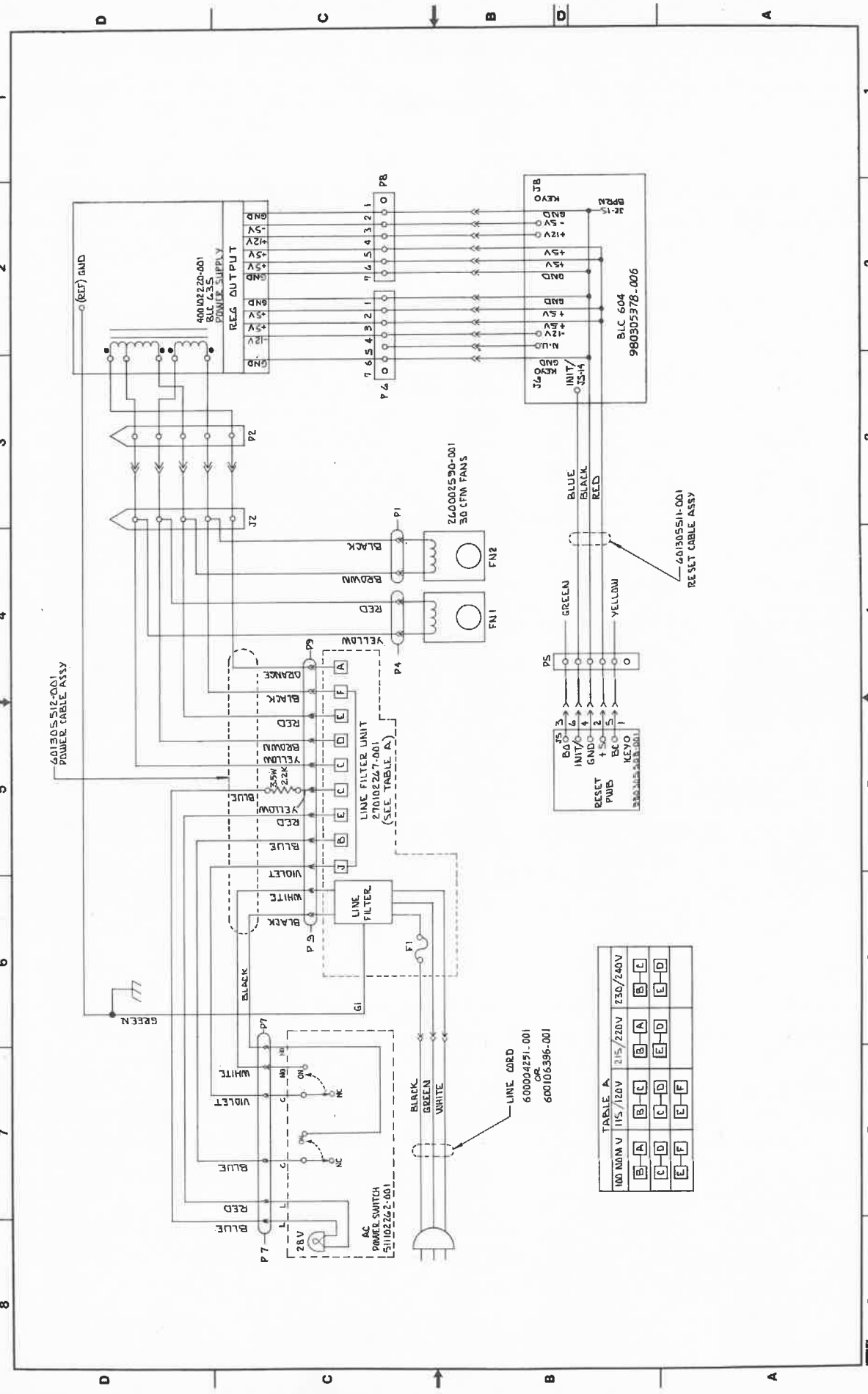


Figure E-1 4-Slot Module Wiring Diagram

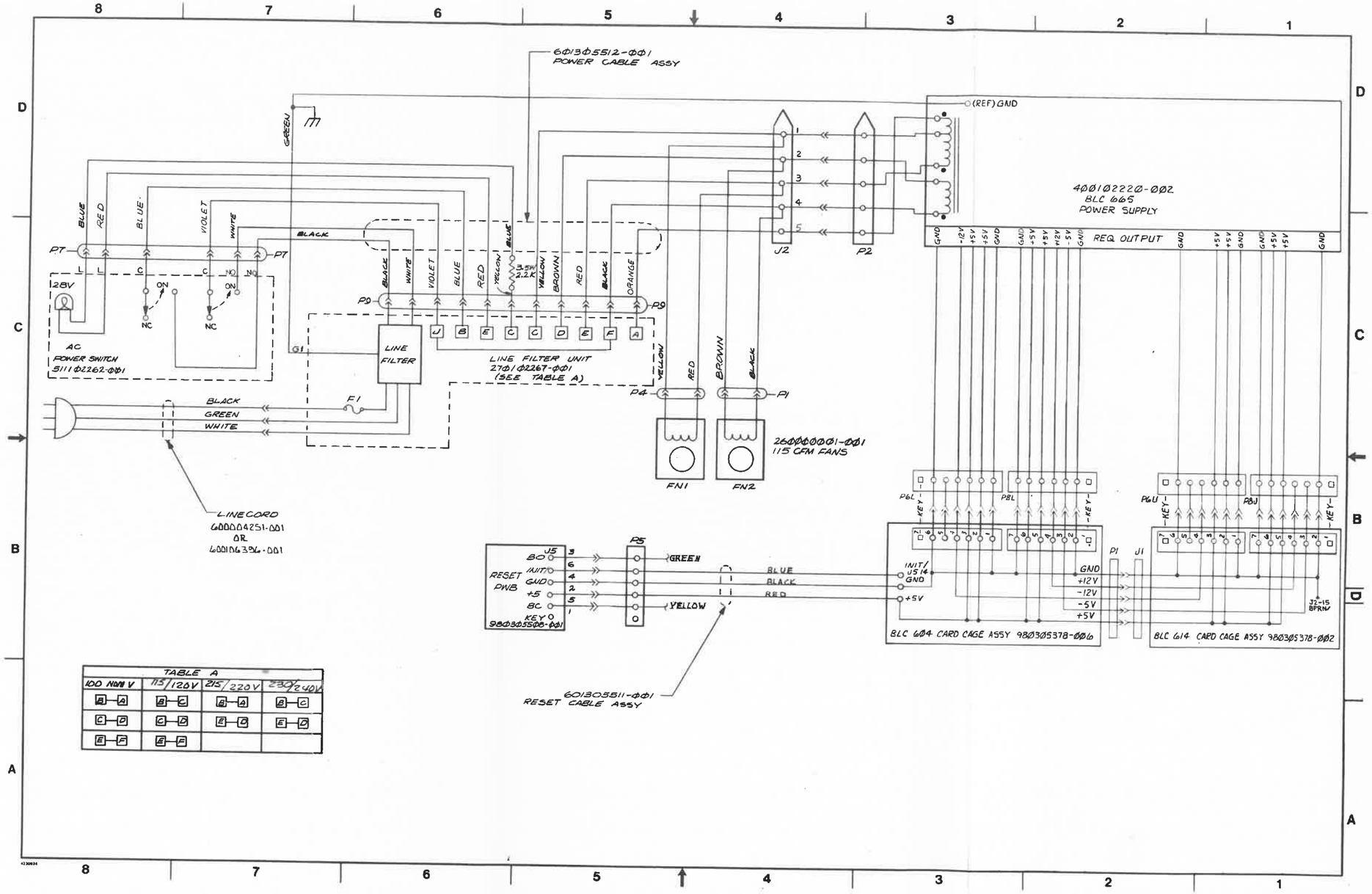
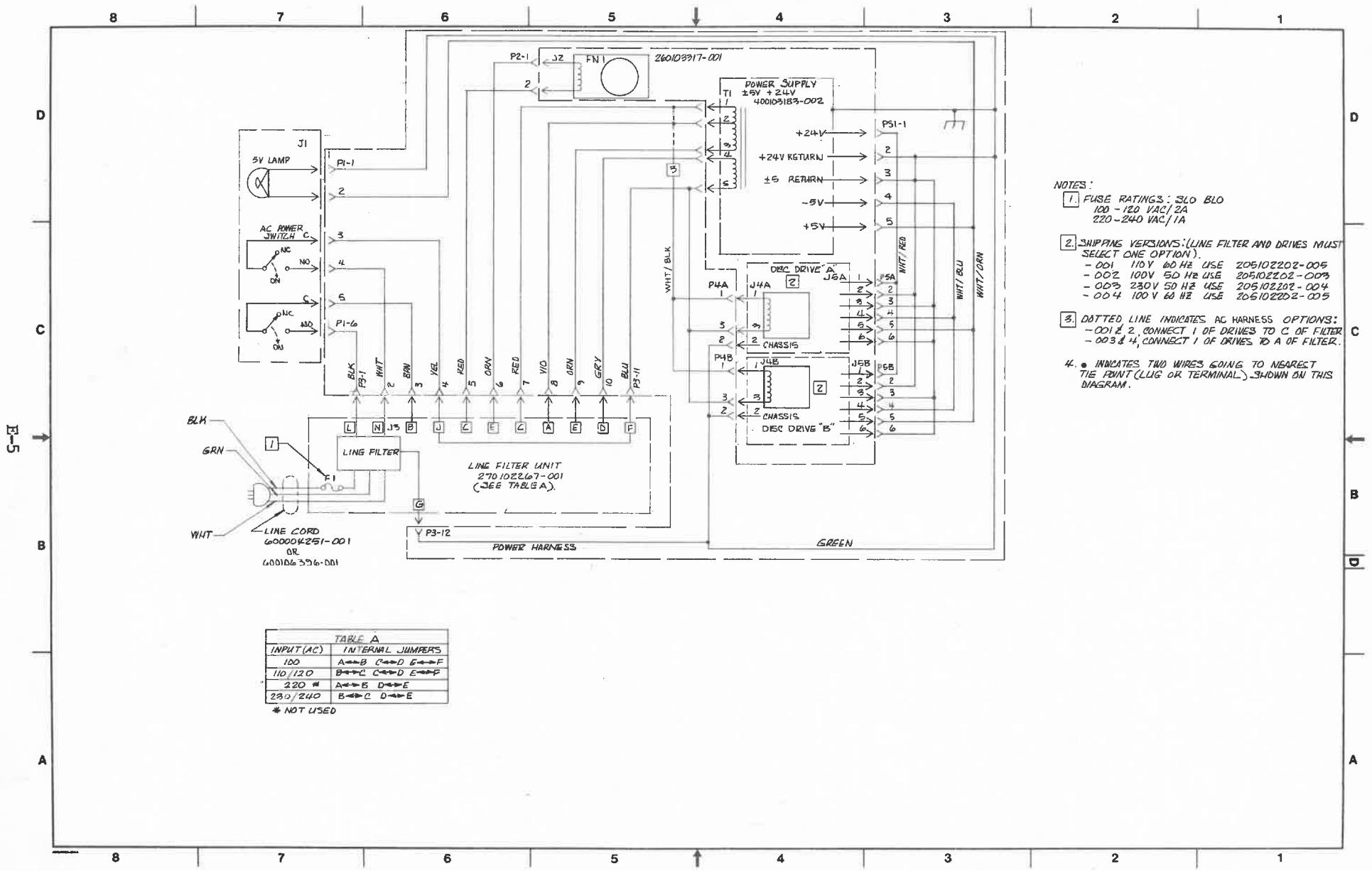


Figure E-2 8-Slot Module Wiring Diagram



NOTES:

1. FUSE RATINGS: SLO BLO
   100 - 120 VAC/2A
   220 - 240 VAC/1A

2. SHIPPING VERSIONS: (LINE FILTER AND DRIVES MUST SELECT ONE OPTION).
   - 001 110V 60 HZ USE 205102202-005
   - 002 100V 50 HZ USE 205102202-003
   - 003 230V 50 HZ USE 205102202-004
   - 004 100 V 60 HZ USE 205102202-005

3. DOTTED LINE INDICATES AC HARNESS OPTIONS:
   - 001 & 2, CONNECT 1 OF DRIVES TO C OF FILTER
   - 003 & 4, CONNECT 1 OF DRIVES TO A OF FILTER.

4. ● INDICATES TWO WIRES GOING TO NEAREST TIE POINT (LUG OR TERMINAL). SHOWN ON THIS DIAGRAM.

TABLE A

INPUT (AC)	INTERNAL JUMPERS
100	A⟷B C⟷D E⟷F
110/120	B⟷C C⟷D E⟷F
220 *	A⟷B D⟷E
230/240	B⟷C D⟷E

* NOT USED

Figure E-3 Flexible Disk Drive Module Wiring Diagram

Appendix F

CABLE ASSEMBLIES

The Cable Assemblies for the MSC-6601/MSC-6605 Rack-Mount Computer Systems are shown on pages F2 through F-7.

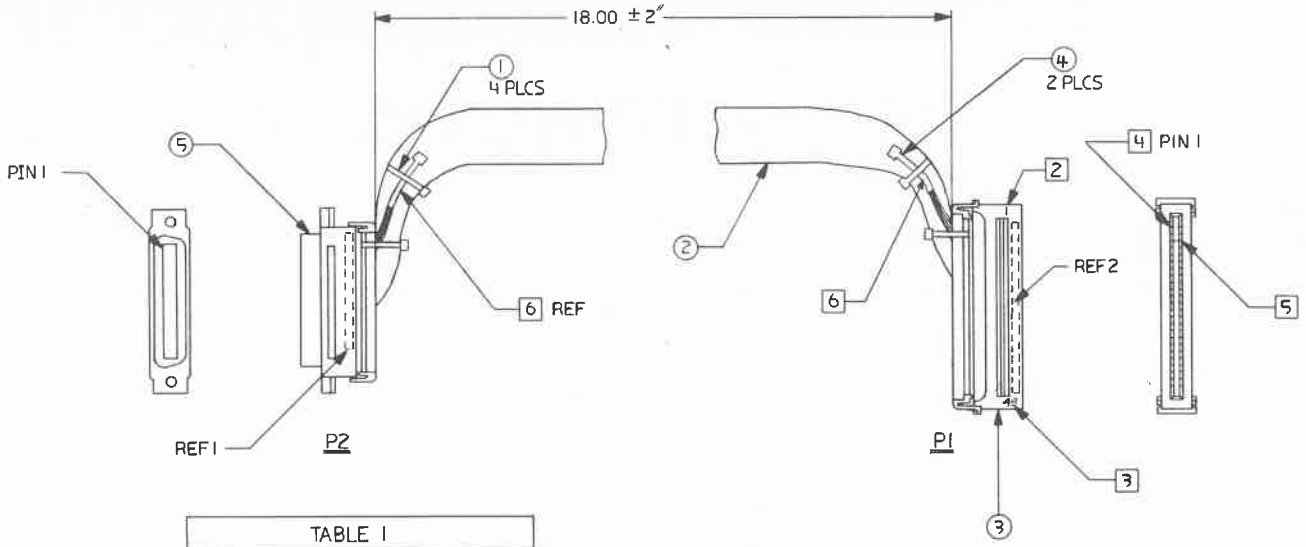
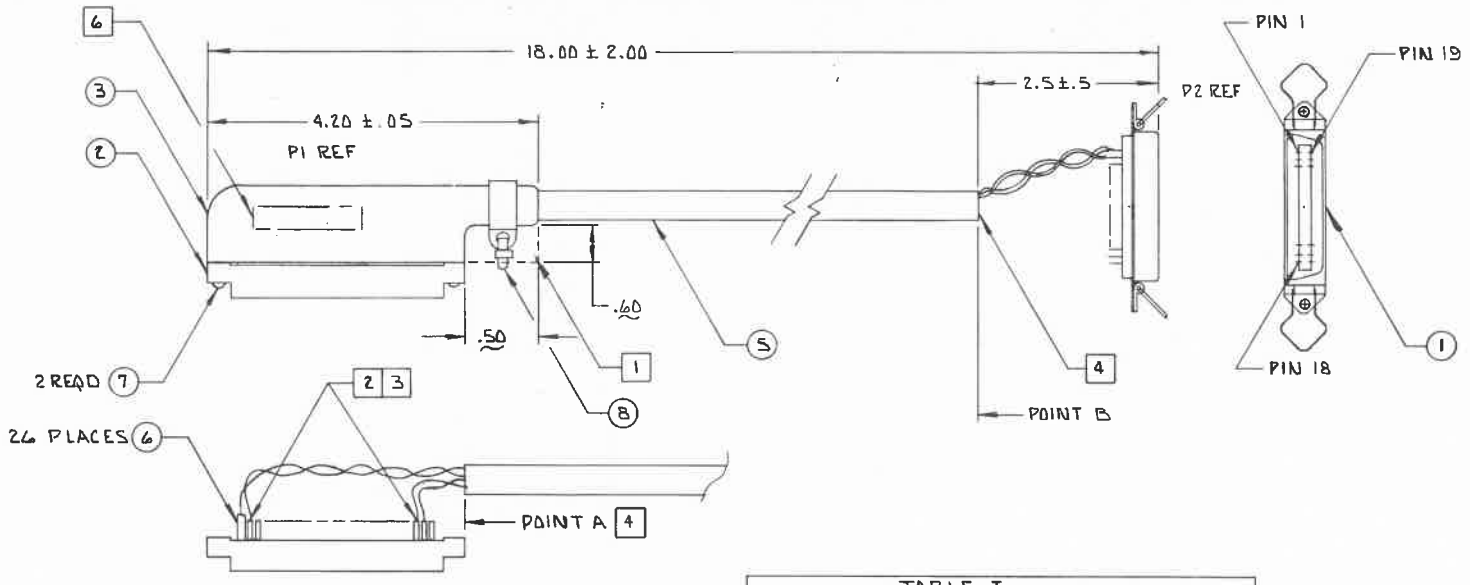


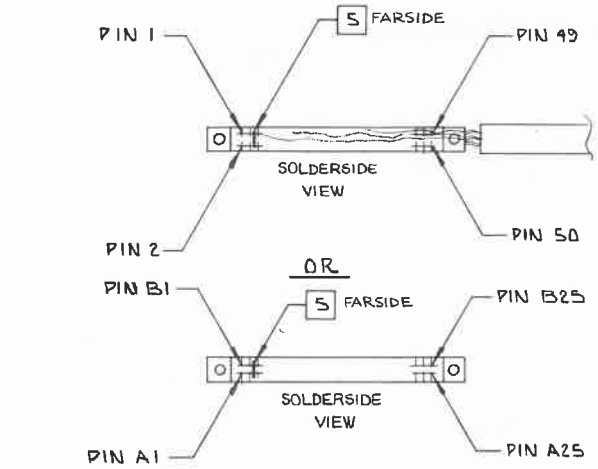
TABLE 1			
PAIR PIN	P1	P2	WIRE COLOR
1	14 13	31 30	BROWN BLACK
2	16 15	1 18	RED BLACK
3	18 17	5 23	ORANGE BLACK
4	20 19	4 22	YELLOW BLACK
5	22 21	3 21	GREEN BLACK
6	24 23	2 20	BLUE BLACK
7	26 25	6 24	VIOLET BLACK
8	28 27	7 25	GRAY BLACK
9	30 29	8 26	WHITE BLACK
10	32 31	9 27	BROWN BLACK
11	38 37	13 –	RED BLACK
12	40 39	12 –	ORANGE BLACK
13	42 41	32	YELLOW BLACK
14	44 43	33 –	GREEN BLACK
15	48 47	11 29	BLUE BLACK

NOTES:
1. Ignore vendor molded pin numbers, use ink stamped pin numbers, 1 and 49, for orientation.

2. Install key between pins 5 and 7.

Figure F-1 Internal Printer Interface Cable





NOTE: Install key supplied with part, between pins 5 and 7 or B3 and B4.

TABLE I

PAIR	P1	P2	WIRE COLOR	LENGTH: +0.1, -0.0 FROM POINT A
1	A24 OR 48 B24, 47	11 29	WHITE GREEN	1.1 INCHES 1.1 "
2	A22, 44 B22, 43	33 —	GREEN RED	1.4 0
3	A21, 42 B21, 41	32 —	BROWN RED	1.5 0
4	A20, 40 B20, 39	12 —	YELLOW RED	1.6 0
5	A19, 38 B19, 37	13 —	ORANGE RED	1.7 0
6	A16, 32 B16, 31	9 27	BLUE RED	2.4 2.4
7	A15, 30 B15, 29	8 26	YELLOW BLACK	2.5 2.5
8	A14, 28 B14, 27	7 25	WHITE BLACK	2.6 2.6
9	A13, 26 B13, 25	6 24	BLUE BLACK	2.7 2.7
10	A12, 24 B12, 23	2 20	BROWN BLACK	2.8 2.8
11	A11, 22 B11, 21	3 21	RED BLACK	2.9 2.9
12	A10, 20 B10, 19	4 22	ORANGE BLACK	3.0 3.0
13	A9, 18 B9, 17	5 23	GREEN BLACK	3.1 3.1
14	A8, 16 B8, 15	1 19	GREEN BLUE	3.2 3.2
15	A7, 14 B7, 13	31 30	WHITE RED	3.3 3.3

Figure F-2 Internal Printer Interface Cable

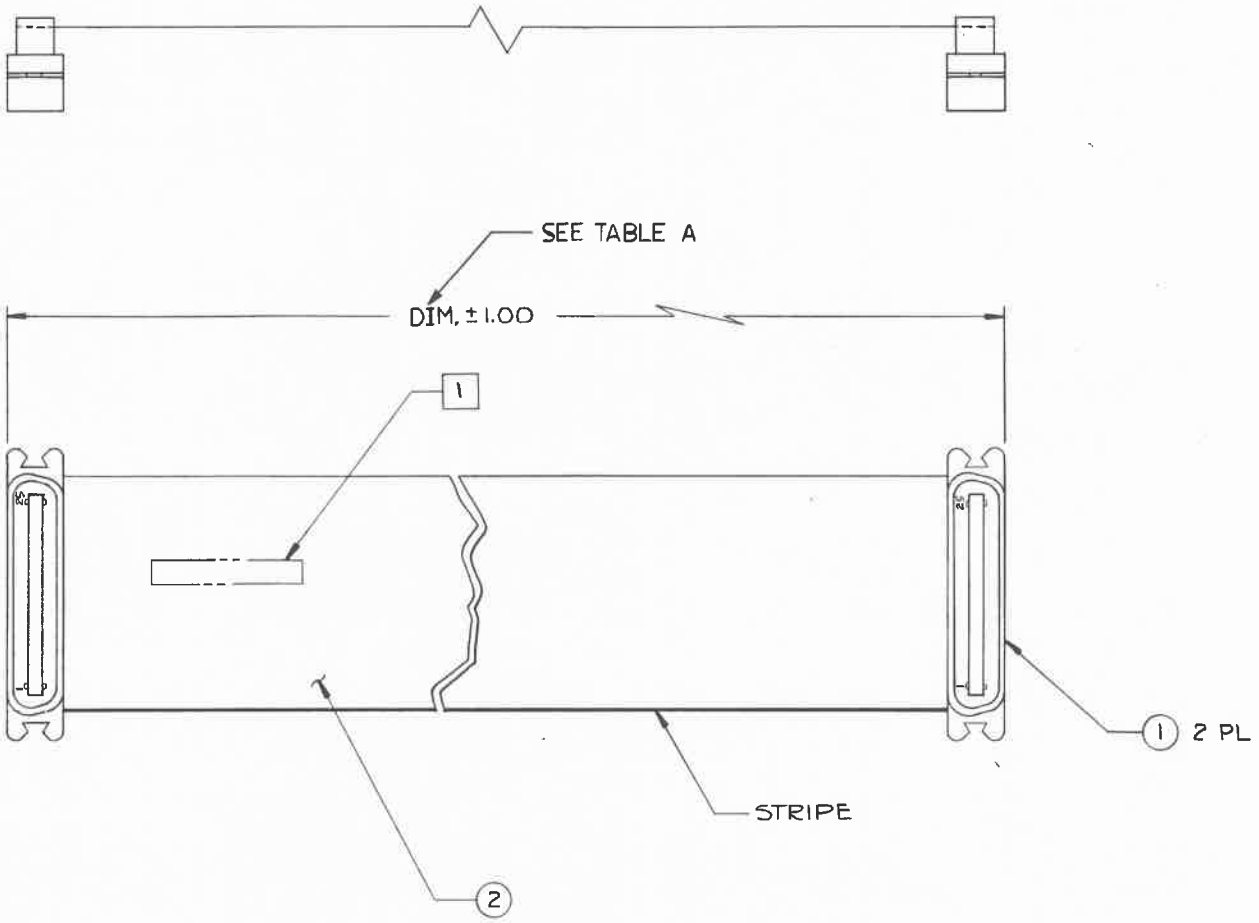
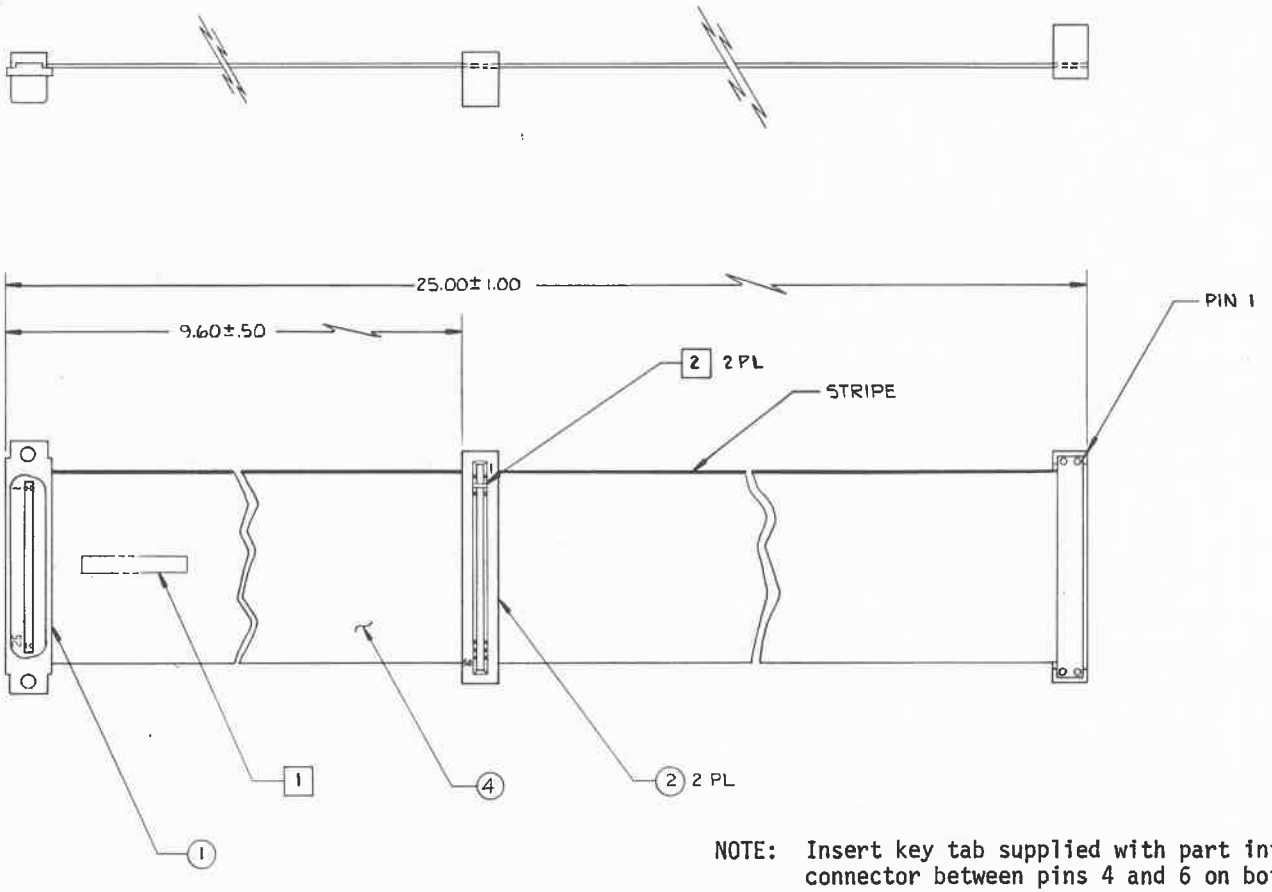
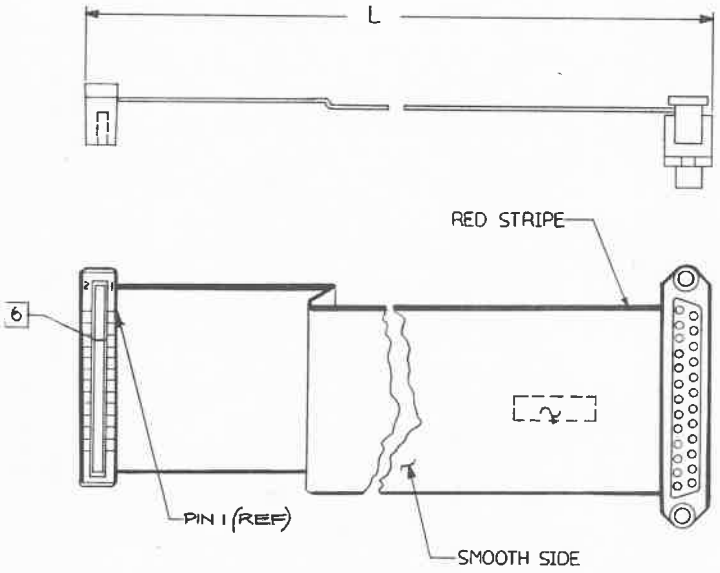


Figure F-3 Inter-Module Signal Cable



NOTE: Insert key tab supplied with part into connector between pins 4 and 6 on both connectors.

Figure F-4 Internal Flexible Disk Drive Module Cable



VERSION	L
-001	28.5 IN.
-002	8.0 IN.
-003	8.0 IN.
-004	12.0 IN

NOTE: Install key between pins 5 and 7.

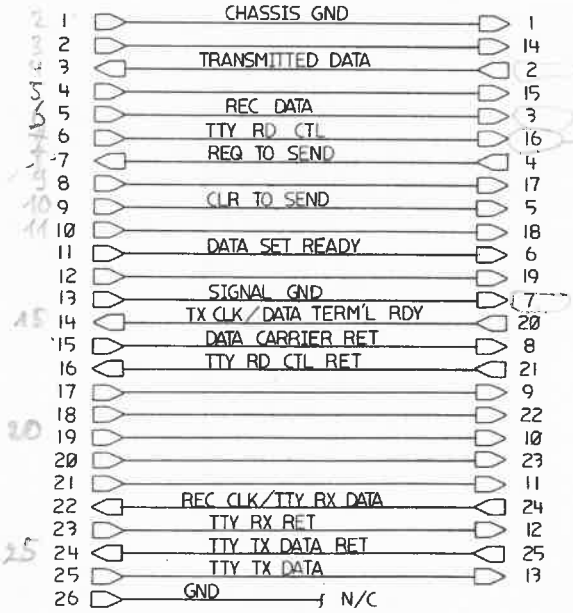
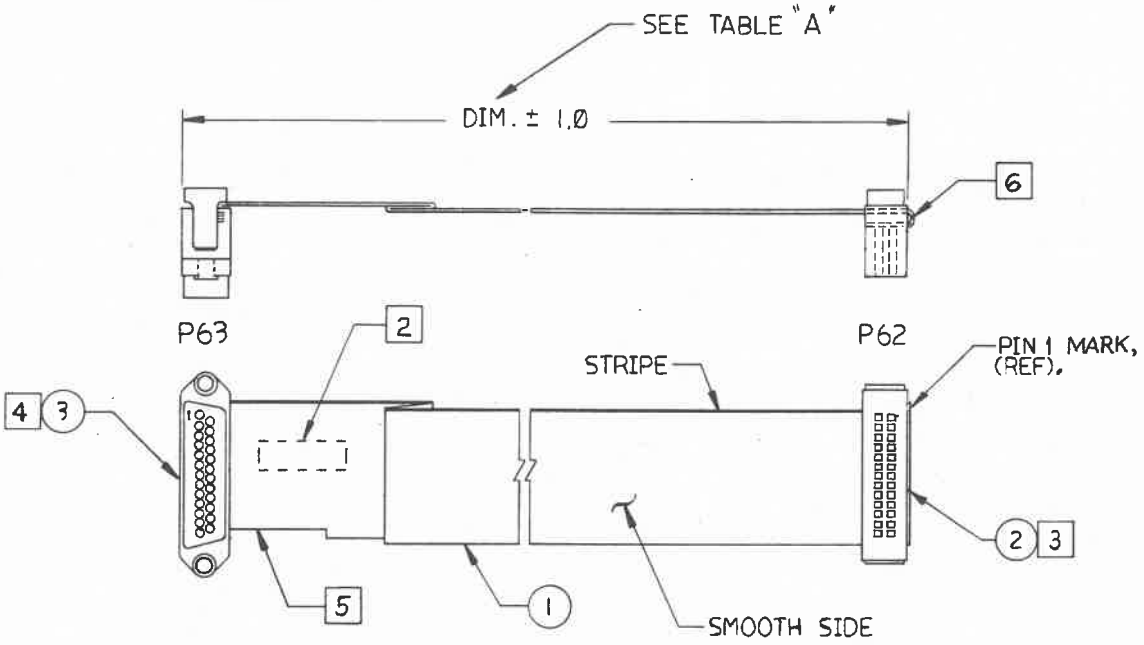


Figure F-5 Internal #1 RS232C Cable

CRT



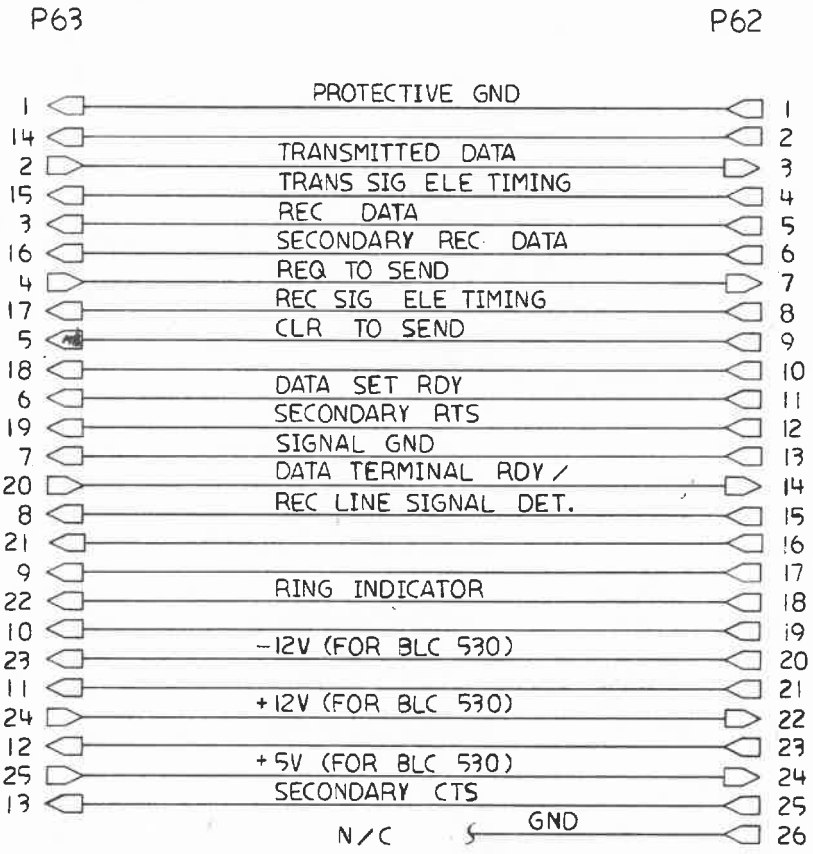


Figure F-6 Internal #2 RS232C Cable

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